Monolithic Memories
INCORPORATED
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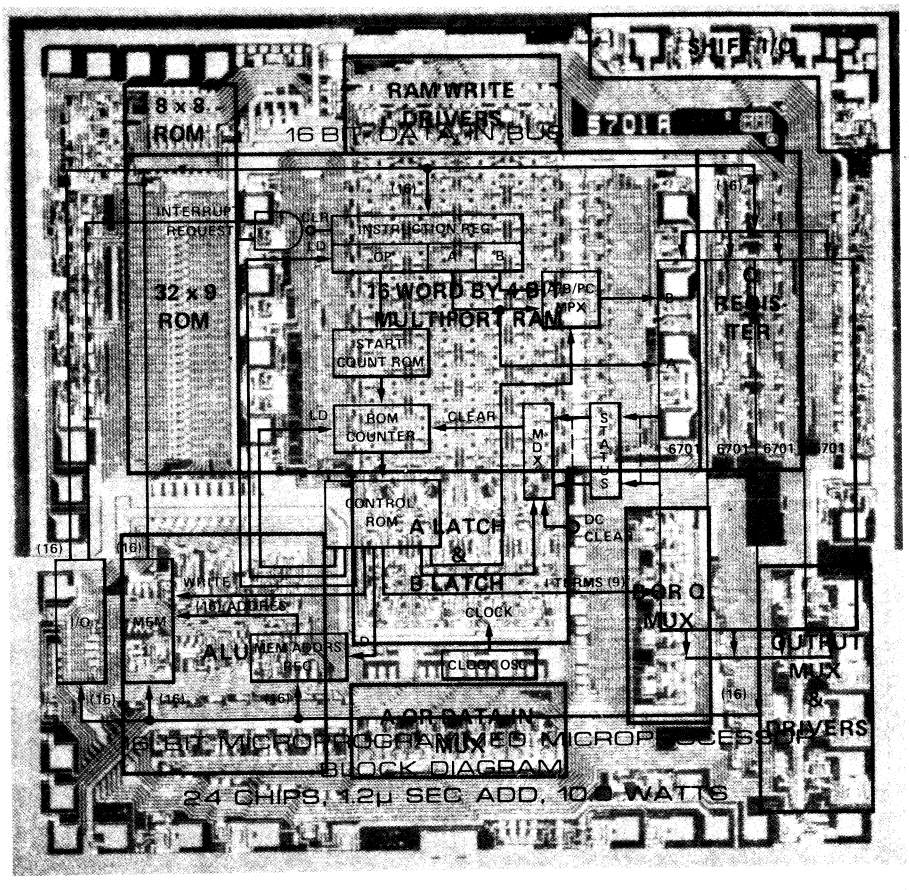

Semiconductor memories
Data
Applications
Reliability Report

Monolithic Memories
INCORPORATED

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1975

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BIPOLAR CHARACTER GENERATORS

(ASC II Encoded)

BIPOLAR RANDOM ACCESS MEMORIES

NEW PRODUCTS

Monolithic Memories is a progressive corporation engaged in the engineering, manufacturing and marketing of semiconductor memory products. Monolithic Memories produces and sells semiconductor memory components as well as advanced semiconductor systems for both military and industrial use. M.M.I. semiconductor memory products are marketed world wide by experienced sales engineers who are responsible for translating customer needs to M.M.I. product capability. A broad range of semiconductor technologies are available to customer for both standard and custom L.S.I. semiconductor products. Monolithic Memories basic charter is to provide timely solutions to its customers memory system needs utilizing advanced forms of semiconductor integration coupled with proven production techniques. The combination of material resources and technical expertise assures M.M.I.'s customers of timley delivery.

The fundamental TTL technology used by M.M.I. has become the industry standard for integrated circuits. TTL is particularly applicable to bipolar memory products since it is considered the most "forgiving or tolerant" process regarding manufacturing variances. The ability to build high complexity memory systems on a single silicon chip is absolutely essential in order to be cost effective.

MANUFACTURING CAPABILITY

The manufacturing equipment and facilities employed by Monolithic Memories represent the most advanced production techniques available. No compromise in equipment performance or facilities arrangement has been tolerated due to the stringent requirements of the LSI semiconductor memory processes. Good facilities and equipment represent only part of the manufacturing equation. Experianced production engineering personnel provide the catalst necessary to meet high volume production schedules.

FACILITIES

Manufacturing operations involving epitaxi, diffusion, photomask exposure, developement, and contact metalisation are performed in a class 100 vertical laminar- flow clean area. This type of clean room is mandatory to produce high complexity, semiconductor, memory products with predictable yield results. All personel in this area are required to wear lint-free clothing at all times. Every precaution has been taken to minimize possible causes of contamination during processing.

The final assembly is accomplished in an extremely clean atmosphere with the most modern equipment available. Every step in the assembly process from chip alloy to final seal is tightly controlled and maintained to ensure built-in quality. The wafer attach and interconnection techniques employed are proven industry standards for high reliability, integrated circuits.

FINAL ELECTRICAL TEST

Monolithic Memories has developed high speed computerized testing systems capable of 100 per cent electrical tests for all specified AC and DC parameters, at higher rates than any commercially available automatic tester. Monolithic Memories *is the only company* that 100 percent tests all AC and dynamic tests on all components, subsystems and systems.

CIRCUIT DEVELOPMENT CAPABILITY

Monolithic Memories design engineering group represents a highly skilled staff capable of quick response to both semiconductor memory and associated custom logic designs. M.M.I. will apply its "know-how" in bipolar L.S.I. to customer custom circuit needs. A complete engineering capability exists to serve changing market demands.

1. Circuit design and analysis.
2. Chip layout, Photomask processing.
3. Product fabrication.
4. Characterization.
5. Prototype, Production delivery.

The organization with Monolithic Memories provides for maximum security of proprietary customer engineering data. Only one or two of the engineers who interface directly with the customer are involved form initial design through final shipment of the finished product. This organization improves communications and provides additional customer confidence in meeting delivery schedules.

SEMICONDUCTOR MEMORY PRODUCT SPECTRUM

TECHNOLOGY

The basic circuit performance required for semiconductor memory products is more demending than other forms of integrated circuits. MMI has a strong position in all major saturated logic technologies. Our approach is to recommend the technology that best fits our customer's system needs. Since no universal integrated circuit technology exists for all memory needs, a broad spectrum of experience in a single supplier is desireable.

The four basic measures of a company's semiconductor capability are Speed, Power Circuit Complexity and Cost. A brief discussion of these parameters is in order. Speed as related to memory products is represented by access time.
Access time is closley related to power dissipation per bit. It is highly desirable to have low access time as well as low power dissipation perbit. PD/Bit $\times$ A_T= P_j/NSEC. (Figure of merit).

MMI offers to its customers the most complete choice of memory products.

PACKAGING

All standard 16, 24 and 40 pin packs are available, including Military Flat Packs.

CUSTOM DEVELOPMENT CAPABILITY

In addition to its line of product, Monolithic Memories will seek custom memory business within the capabilities of the bipolar memory technology. This capability extends from component to subsystem, to wire wrapped system with supporting power supplies and mother boards.

We hope that this Data book will be a valuable aid in choosing devices for your next advanced range of equipments.

BIPOLAR WAFER FABRICATION FLOW DIAGRAM

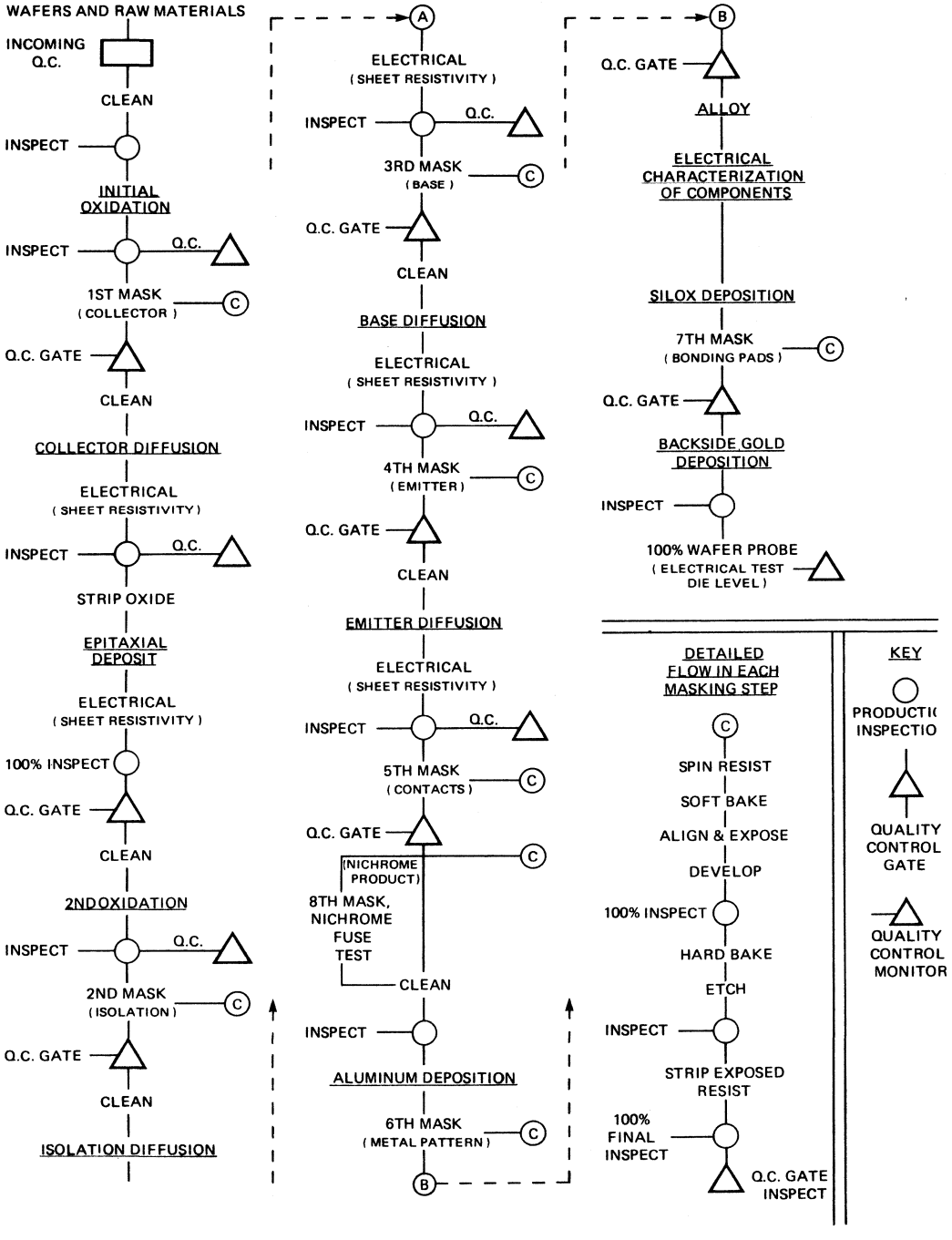


Fig 1

ASSEMBLY - TEST FLOW DIAGRAM

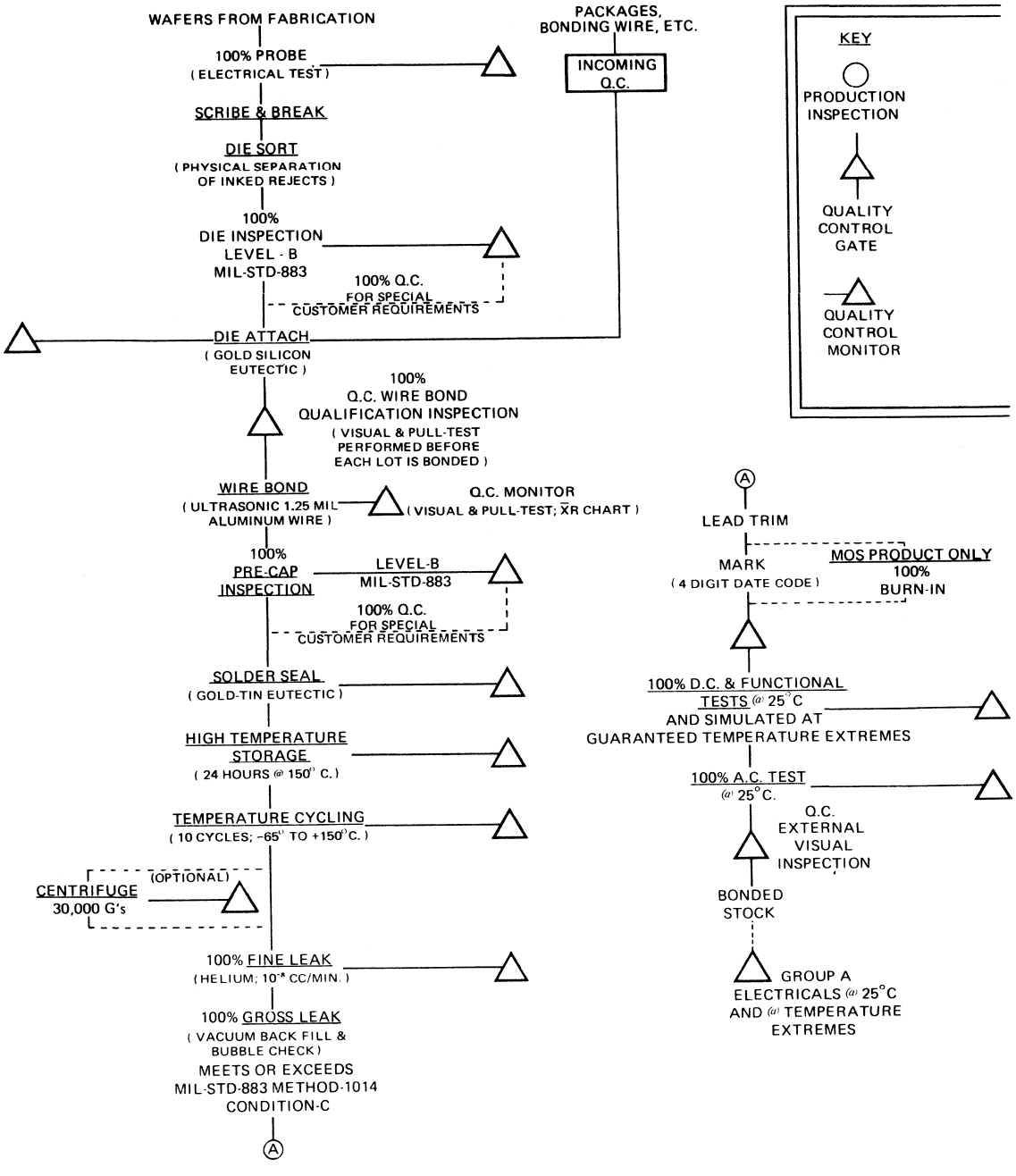


Fig 2

1024 BIT BIPOLAR (256x4) ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

5300/6300
5301/6301

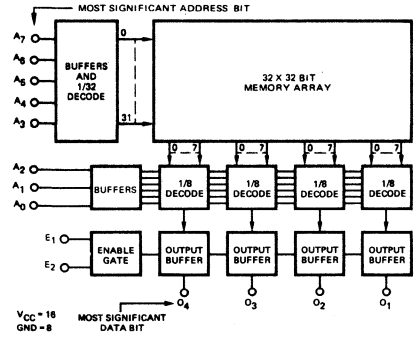
Monolithic Memories
INCORPORATED

PRODUCT FEATURES:

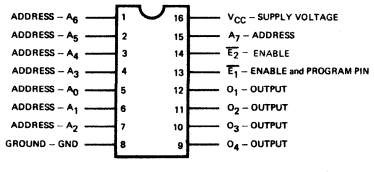
- **Field Programmable with Simple Programming Procedure**
- **Pin Compatible with Mask Programmable 5200/6200/ H5201/H6201**
- **Fast Programming Time — Average of 5 ms/Bit**
- **Standard Packaging — 16 Pin DIP**
- **Fully Decoded — On Chip Address Decoding**
- **DTL and TTL Compatible**
- **Three-State or Open Collector Outputs**
- **Special On Chip Circuitry Permits V_{OL} Testing before Programming**

	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
6300		X		X
6301		X	X	
5300	X			X
5301	X		X	

BLOCK DIAGRAM: 256 Words X 4 Bits Memory



PIN CONFIGURATION



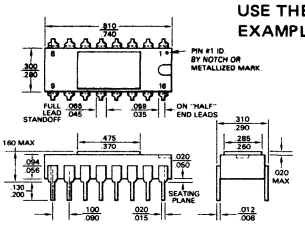
To enable the device $\overline{E}$, and $\overline{E}_2$ must be low.

PACKAGE OUTLINE

16 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/ watt

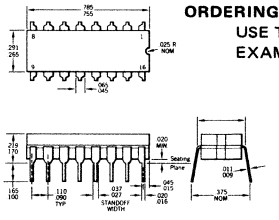
ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6300D



16 Pin Ceramic (CERDIP)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 75°C/watt

ORDERING INFORMATION
USE THE SUFFIX J
EXAMPLE 6300 J



NOTE: Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt for both packages.

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MARCH 1974

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	–0.5 to 7 V	Pin 6 Voltage During Vol Checks	13 V
Input Voltage (except Pins 6 and 13)	–1.0 to 5.5 V	Program Pin Voltage (Pin 13) During Programming	35 V
Output Current	100mA	Output Voltage During Programming	27 V
Input Current	–20 to 5mA	Programming Duty Cycle	25% MAX.
Storage Temperature	–65 to +150°C	Stresses above or extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.	

D.C. CHARACTERISTICS Unless otherwise indicated, all limits for the 6300/6301 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5300/5301 are guaranteed for 5 V ±10% in a free air temperature of –55 to 125°C

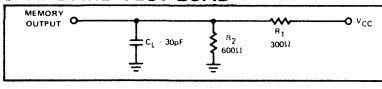
PARAMETER		CONDITIONS	5300/5301			6300/6301			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V		–1.0	–1.6		–1.6	–1.6	mA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			40			40	μA
I_{RB}	Input Leakage Current, All Inputs Except Pin 13	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
I_{RB}	Pin 13 (Program Pin) Only	V_{CC} = Max, V_{RB} = 4.5 V			1			1	mA
		V_{CC} = Max = V_{RB}			20			20	mA
V_{OL}	Low Level Output Voltage See Note 2 Below	V_{CC} = Min, I_{OL} = 10 mA		.35	0.45				V
		V_{CC} = Min, I_{OL} = 16 mA					.35	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, All Inputs GRD (worst case) All Outputs Open		80	120		80	120	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current 5300/6300 Only	V_{CC} = Max, V_{CEX} = 2.40 V High Stored or Disabled			100			100	μA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_L = –5.0 mA		–1.0	–1.5		–1.0	–1.5	V
C_L	Input Capacitance	V_{CC} = 5.0 V, V_L = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF
THREE STATE PARAMETERS – 5301/6301 ONLY									
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5 V	–20	–50	–90	–20	–50	–90	mA
I_{HZ}	Output Leakage	V_{CC} = Max, V_O = .45 to 2.40 V Chip Disabled			±100			±100	μA
V_{OH}	Output Voltage "High"	I_O = –2.0 mA for the 6301 I_O = –900 μA for the 5301	2.4	3.2		2.4	3.2		V

1. Typical values are measured at 5.0 V and 25°C.
2. Unprogrammed P.ROMS will have all outputs high. V_{OL} can be tested by taking pin 6 to 11 V (less than 10 mA must be supplied) and pin 5 to a voltage between 2.4 and 5.0 V and enabling the chip. This procedure turns on all four outputs and permits V_{OL} tests.

A.C. CHARACTERISTICS With Standard Load

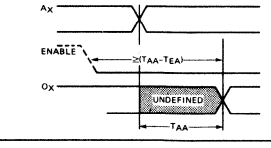
PARAMETER	SYMBOL	FIGURE	5300/5301 5.00 V, 25°C		6300/6301 5.00 V, 25°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	1	10	60	10	60
Enable Access Time	T_{EA}	2	5	30	5	30
Enable Recovery Time	T_{ER}	2	5	30	5	30
5301/6301 ONLY						
Chip Enable to Low Impedance Delay	T_{ON}		5		5	
Chip Enable to High Impedance Delay	T_{OFF}			25		25

STANDARD TEST LOAD



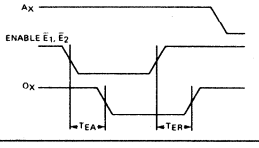
Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 15 mA and 30 pF as given in std. load

Fig. 1 ADDRESS ACCESS TIME



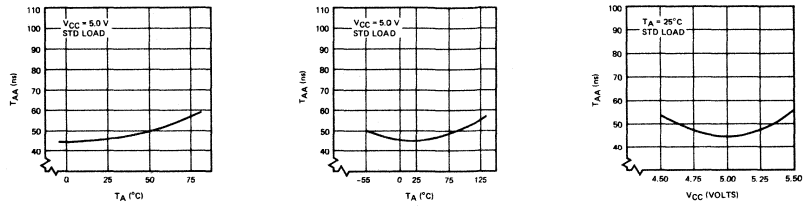
Ax = Any Address
Ox = Any Output

Fig. 2 ENABLE ACCESS TIME AND RECOVERY TIME



ELECTRICAL PARAMETERS

CURVES OF TYPICAL DEVICES



Note: The T_{EA} parameter typically varies from 21 to 33 ns for any device type over the voltage and temperature range of 5 V ±10%, −55 to 125° C.

PULLUP RESISTOR SELECTION FOR 5300 AND 6300

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 16 mA for the 6300
10 mA for the 5300
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four 6300 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 16 mA

$$R_L(\text{max}) = \frac{V_{CC}-2.40\text{ V}}{M(100\,\mu A)+N(I_R)} \qquad R_L(\text{max}) = \frac{5.0-2.4\text{ V}}{4\,(100\,\mu A)+3\,(40\,\mu A)} = 5000\text{ ohms}$$

$$R_L(\text{min}) = \frac{V_{CC}-0.45\text{ V}}{I_{OL}-N(I_F)} \qquad R_L(\text{min}) = \frac{5.0-0.45\text{ V}}{16\text{ mA}-3(1.6\text{ mA})} = 406\text{ ohms}$$

THREE-STATE OUTPUT – See Figures A and B

FIGURE A
THREE-STATE OUTPUT

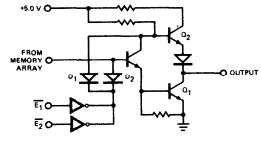
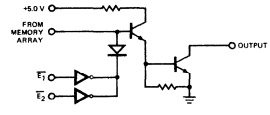


FIGURE B
OPEN COLLECTOR OUTPUT



The three-state output of the 5301/6301 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip enable is low D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment, up to 21 outputs of the 6301 or 10 outputs of the 5301 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

MEMORY OPERATION

The memory is addressed with inputs A_0 through A_7 which select one of 256 words. A four bit parallel readout is available for each word on outputs O_1 to O_4. To enable the outputs for a readout, both enables $\overline{E}_1$ and $\overline{E}_2$ must be low. If either enable, or both, is high, the outputs are held off permitting wire"OR"ing of three-state or open collector outputs of several packages. The use of the enables permits expansion to greater than 256 words.

PROGRAMMING INFORMATION

PROGRAMMING INSTRUCTIONS

1) DEVICE DESCRIPTION

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. There are 1024 fusible links on the chip. Programming equipment can be obtained from Monolithic Memories Inc.

2) PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_7, a V_{CC} of 5.50 V is applied or left applied, and the program pin (Enable $\overline{E}_1$) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

3) ENABLE $\overline{E}_2$

Enable $\overline{E}_2$ (pin 14) is a logic enable and is not used during programming. It may be high, low or open during programming. When checking that an output is programmed (which is called verification) enables $\overline{E}_1$ and $\overline{E}_2$ must be low to activate the device. Since $\overline{E}_2$ must be low during verification and the state is irrelevant during programming, the simplest procedure is to ground $\overline{E}_2$ during programming and verification.

4) TIMING

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate.
The programming pulse applied to the output pin must have 10 microseconds or slower rise time to avoid capacitively coupling the output signal into the base of the output transistor, causing it to turn on and go into avalanche breakdown. This coupling would occur during the low to high transition of the output pin's programming pulse through the output transistors' collector to base capacitance. Similar consideration limit the rise time of the program pin. Fall times are not critical.

5) VERIFICATION

After programming a device, it can be checked for a low output by taking both enables low. Since we are checking for a programmed high resistance fusible link and must guarantee operation at minimum voltage, maximum sink current, and cold temperature, the device must be required to sink 12 mA at 4.20 V V_{CC} at room temperature to guarantee a fully programmed link.

6) BOARD PROGRAMMING

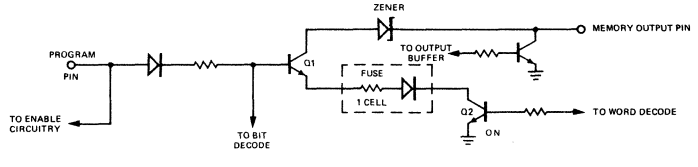
Units may be programmed at the board level by bringing the program pin of each package to the card connector. To program a particular package "A", the program pin of package A and one output of package A, which may or may not be "OR" tied to other packages, are taken to the required programming voltage. An alternate procedure is to tie the enable and outputs together as required by the system function and only apply V_{CC} to the device to be programmed. The number of units soldered on a board should be consistent with expected programming yields to avoid rework.

7) UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. **UNITS RETURNED TO MMI AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULDN'T BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

OPERATION

PROGRAMMING EQUIVALENT CIRCUIT FOR ONE MEMORY OUTPUT



The word decode circuitry selects transistor Q_2 to be turned on, and the bit decode circuitry allows the base of Q_1 to rise. 1023 other fuses are half selected or not selected. The program pin supplies base drive to Q_1 and the output pin supplies collector current to Q_1 so that Q_1's emitter can deliver the required current to open the fusible link.

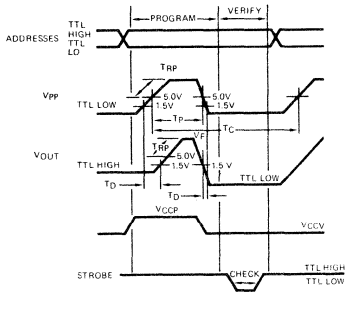
FIGURE 3

PROGRAMMING INFORMATION

PROGRAMMING PARAMETERS – Do Not Test These Limits or You May Program The Device.

SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS MIN.	LIMITS TYPICAL OR OPTIMUM	LIMITS MAX.	UNITS
I_{pp}	Current into Program Pin During Programming, Before and After Fuse Has Blown	V_{CC} = 5.50 V V_{out} = 5.0 V to 25 V V_{pp} = 4.50 V		0		mA
		V_{pp} = 29 V		77		mA
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{pp} = 29 V, V_{CC} = 5.50 V V_{out} = 9.0 V		0.1		mA
		V_{out} = 20 V		16		mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{pp} = 29 V, V_{out} = 20 V V_{CC} = 5.50 V		0.1		mA
T_{RP}	Rise Time of Program Pulse Applied to the Data out or Program Pin From 5 V to 20 V		10.0	20±10	100	μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
V_{CCV}	V_{CC} Required During Verification	Both Chip Enables Low	4.10	4.20	4.30	V
I_{OLV}	Output Current Required to Guarantee a Fully Programmed Link	T_A = 25°C, V_{CC} = 4.20 V	12			mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	$\frac{T_P}{T_C}$			25	%
V_{pp}	Required Programming Voltage on Program Pin		28		34	V
V_{out}	Required Programming Voltage on the Output Pin		20		26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{pp} = 33 V V_{out} = 25 V V_{CC} = 5.50 V	150			mA
T_p	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		0.040		300	ms
T_D	Required Time Delay Between Disabling the Memory Output and Application or Removal of the Output Programming Pulse (see Item 4, page 4)	Measure at 1.5 V Levels	100			ns

TIMING



SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY

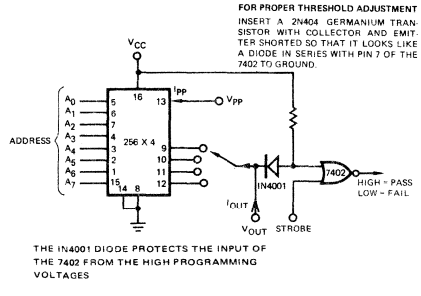


FIGURE 4

PROGRAMMING INFORMATION

PROGRAMMING SPEED

Most fuses will blow on the rise time of the pulse and in less than 10 microseconds. Some fuses however, will require the thermal energy required by higher programming voltages and wider programming pulse widths (up to 200 milliseconds) to open.

In simple programming schemes where the programming time is not critical the wider pulses can be used exclusively. In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to give maximum thruput (less than 3 seconds per device on the average) and programming yield. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	DURATION	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 4	40 μs	29 V	20 V
5 to 8	40 μs	33 V	25 V
9 to 12	20 ms	33 V	25 V
13 to 16	200 ms	33 V	25 V

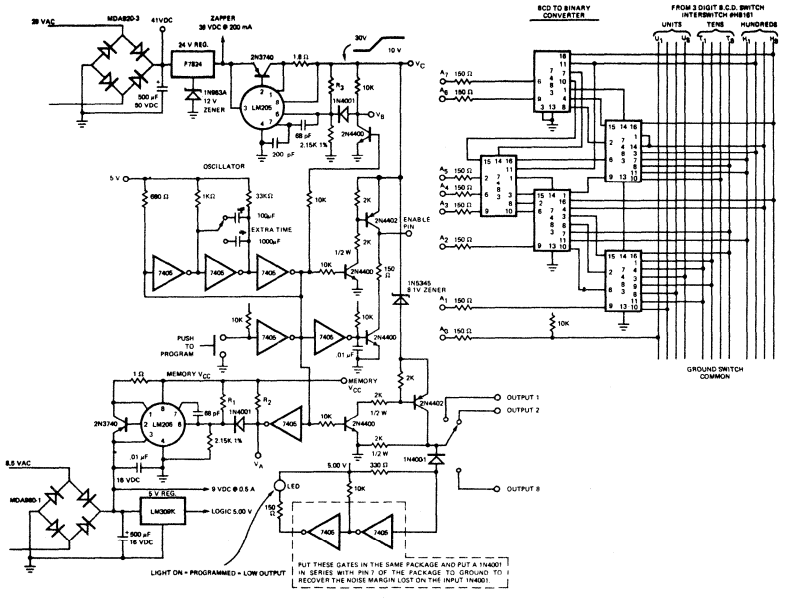
PROGRAMMER DESCRIPTION

Figure 5 below shows the circuitry required to build a simple manual programmer. The operator with this programmer dials in the memory address to be programmed on a three digit thumbwheel switch and selects the output to be programmed or readout on a 4 position rotary switch. Pushing the program button will open the nichrome link at the selected address. When the program button is released the memory data is displayed on an LED.

OPERATION

Five 7483's are used to convert from BCD to binary addresses. An LM205 is used to control the device V_{CC} and vary it from 4.20 to 5.50 V depending upon whether V_A is high or low. V_A and V_B are controlled by the oscillator which is turned on when the program button is pushed. V_A and V_B vary the device V_{CC} and programming voltage by changing the resistor divider values on the LM205 which set the output voltage. Two oscillator speeds can be selected by a two position switch.

MANUAL PROGRAMMER



NOTES:

1. Adjust R_1 and R_2 so that the memory V_{CC} is 4.150 to 4.250 V quiescent and 5.450 to 5.550 V when the program button is pushed. $R_1 \approx 5K$. $R_2 \approx 15K$.
2. Adjust R_3 for 30 to 31 V on V_C when the program button is pushed. $V_C \approx \frac{R_3\,(K\Omega)}{2.15k}(1.7\text{ V})$ SO $R_3 \approx 37K$
3. Use Thermalloy heat sink #6166B on both 2N3740 transistors.

REQUIRED INFORMATION FOR MMI TO PROGRAM TO YOUR TRUTH TABLE

TRUTH TABLES

MMI can program devices at our facility from MMI truth table forms (available on request). For customers desiring to make their own forms, an example is shown below:

		OUTPUTS			
WORD	PIN → 9	10	11	12
NUMBER	O_4	O_3	O_2	O_1
0	H	H	H	L
1	L	H	L	H
.	.	.	.	.
.	.	.	.	.
255	L	H	H	H

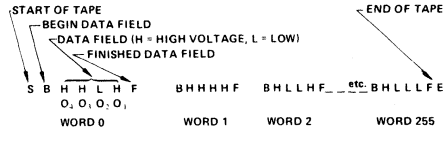
Note: A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pins, so for example, word 255 = HHHHHHHH.

PAPER TAPE FORMAT

Truth tables can also be sent to MMI in an ASCII tape format. Information can be sent to us by air mail or TWX 910-339-9224. The tape reading equipment at MMI only recognizes ASCII characters S, B, H, L, F and E and interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to word 255.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is $0_4, 0_3, 0_2, 0_1$, not $0_1, 0_2, 0_3, 0_4$.

A typical list of charaters and their machine interpretations are shown below:



The required heading information at the beginning of the tape is as follows:

CUSTOMERS NAME AND PHONE _____ TRUTH TABLE NUMBER _____

CUSTOMERS TWX NUMBER _____ NUMBER OF TRUTH TABLES _____

PURCHASE ORDER NUMBER _____ TOTAL NUMBER OF PARTS _____

MMI PART NUMBER _____ NUMBER OF PARTS OF EACH TRUTH TABLE _____

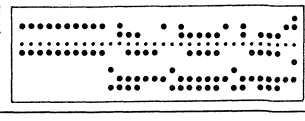
CUSTOMER SYMBOLIZED PART NUMBER _____ 25 BELL OR RUBOUT CHARACTERS _____

An example is shown below:

BLARNEY ELECTRONICS 408-735-8104
TWX 911-338-9225
P0142
6300
0431
12
1
3
3

SBLLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF BLLLLF
BLLLLF BLHLHF BLLHHF BHHHLF BHHLLF BLLHHF BHHLLF BLLHHF BLHLHF

8 level TWX

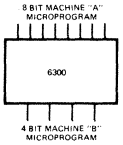


APPLICATIONS

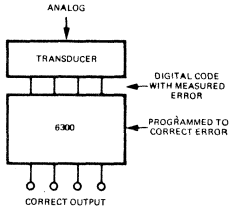
GENERAL

The P.ROM was designed for situations which require a fast turnaround on bit patterns. The device permits patterns to be changed in the field in minutes. The pin and performance compatibility with the mask programmable 256 x 4 ROM permits fast prototyping and the economic advantages of mask made ROM. The interchangeability and side by side operation of the ROM and P.ROM offers an effective means of customizing a small portion of a machine, or permitting engineering changes, or eliminating field stocking of mask programmable ROMs.

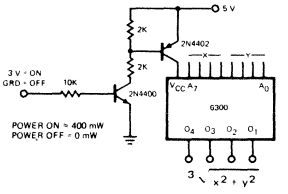
EMULATION



TRANSDUCER ERROR CORRECTION

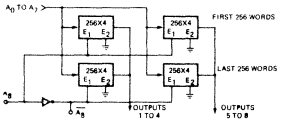


LOW POWER FUNCTION GENERATION

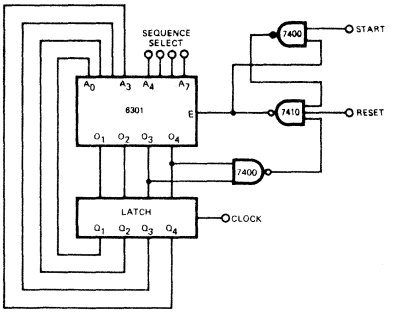


MEMORY EXPANSION 512 X 8 SYSTEM

The highest order address (A_8) is used in conjunction with the chip enables to select either the first 256 words (when A_8) is low) or the last 256 words (when A_8 is high). The corresponding outputs of the packages in the same column are OR tied for the 8 bit readout required.



SEQUENCE GENERATOR



ADDRESS	A_7	A_6	A_5	A_4	SEQUENCE NO.
0 TO 15	L	L	L	L	1) SERVICE TELETYPE
16 TO 31	L	L	L	H	2) SERVICE PRINTER
.		.			.
.		.			.
.		.			.
239 TO 255	H	H	H	H	16) SERVICE TAPE UNIT

The enable is used to define a known starting point since when it is high the memory outputs are high regardless of the programmed code.

RANDOM LOGIC REPLACEMENT

$F1 = (\overline{A}BCD + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}) \cdot \overline{E}\overline{F}\overline{G}H$

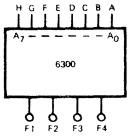
INTERPRETATION:

F1 is high if address 14, 13, 11 or 7 is selected

$F2 = (\overline{A}BCD + BC\overline{D}) \cdot \overline{E}\overline{F}\overline{G}H$

INTERPRETATION:

F2 is high if address 12, 7 or 6 is selected



F3 = E·F·G·H PLUS 1

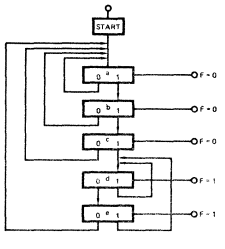
F4 = E·F·$\overline{G}$·H MINUS 1

COMBINATION LOCK OR SEQUENCE DETECTOR

Design a circuit which after initially set to zero, will go to 1 if 3 or more consecutive 1's appear on the input. It should remain at logical 1 until two consecutive logical 0's appear.

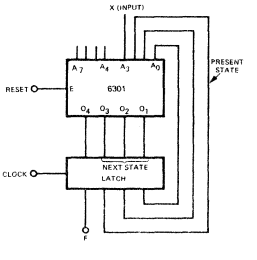
Assign machine states a thru e to the five possible states of the system and call the output F and the input X.

FLOWCHART



STATE TABLE

PRESENT STATE	NEXT STATE X = 0	NEXT STATE X = 1	OUTPUT F OF PRESENT STATE
a	a	b	0
b	a	c	0
c	a	d	0
d	e	d	1
e	a	d	1



2048 BIT BIPOLAR (512 x 4) ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

5305/6305
5306/6306

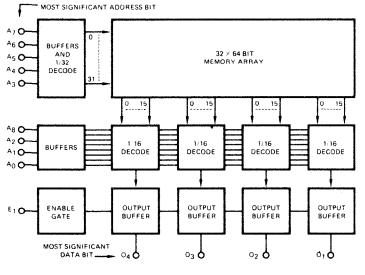
Monolithic Memories
INCORPORATED

PRODUCT FEATURES:

- Field Programmable with Simple Programming Procedure
- Pin Compatible with Mask Programmable 5205/6205 and 1024 Bit (256x4) ROMs and P.ROMs
- Fast Programming Time — Average of 5 ms/Bit
- Standard Packaging — 16 Pin DIP
- Fully Decoded — On Chip Address Decoding
- DTL and TTL Compatible
- Three-State or Open Collector Outputs
- Special On Chip Circuitry Permits V_{OL} Testing before Programming

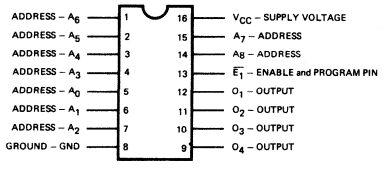
	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
6305		X		X
6306		X	X	
5305	X			X
5306	X		X	

BLOCK DIAGRAM: 512 Words X 4 Bits Memory



V_{CC} = 16
GND = 8

PIN CONFIGURATION



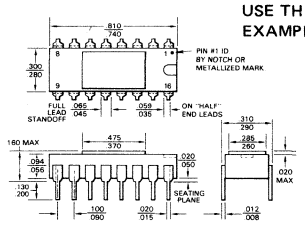
To Enable The Device $\overline{E}_1$ Must Be Low.

PACKAGE OUTLINE

16 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/ watt

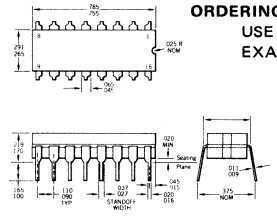
ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6305D



16 Pin Ceramic (CERDIP)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 75°C/watt

ORDERING INFORMATION
USE THE SUFFIX J
EXAMPLE 6305J



NOTE: Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt for both packages.

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

MARCH 1974

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V	Pin 6 Voltage During Vol Tests	13 V
Input Voltage (Except Pins 6 and 13)	−1.0 to 5.5 V	Program Pin Voltage (Pin 13) During Programming	35 V
Output Current	100 mA	Output Voltage During Programming	27 V
Input Current	−20 to 5 mA	Programming Duty Cycle	25% MAX.
Storage Temperature	−65 to +150°C	Stresses above or extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.	

D.C. CHARACTERISTICS Unless otherwise indicated, all limits for the 6305/6306 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5305/5306 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C

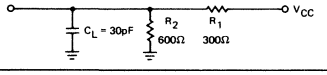
PARAMETER		CONDITIONS	5305/5306			6305/6306			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V		−1.0	−1.6		−1.0	−1.6	mA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			40			40	µA
I_{RB}	Input Leakage Current, All Inputs Except Pin 13.	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
	Pin 13 (Program Pin) Only	V_{CC} = Max, V_{RB} = 4.5 V			1			1	mA
		V_{CC} = Max, V_{RB} = 5.5 V			20			20	mA
V_{OL}	Low Level Output Voltage See Note 2 Below	V_{CC} = Min, I_{OL} = 10 mA		.35	0.45				V
		V_{CC} = Min, I_{OL} = 16 mA					.35	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, All Inputs GRD (worst case) All Outputs Open		80	130		80	130	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current (Open Collector Devices Only)	V_{CC} = Max, V_{CEX} = 2.40 V High Stored or Disabled			100			100	µA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA		−1.0	−1.5		−1.0	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF
THREE STATE PARAMETERS — 5306/6306 ONLY									
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5 V	−20	−50	−90	−20	−50	−90	mA
I_{HZ}	Output Leakage High Impedance State	V_{CC} = Max, V_O = 0.45 V to 2.40 V Chip Disabled			±100			±100	µA
V_{OH}	Output Voltage "High"	I_O = −2.0 mA for the 6306 I_O = −900 µA for the 5306	2.4	3.2		2.4	3.2		V

1. Typical values are measured at 5.0 V and 25°C.
2. Unprogrammed P. ROMS will have all outputs high. V_{OL} can be tested by taking pin 6 to 11 V (less than 10 mA must be supplied) and enabling the chip. This procedure turns on all four outputs and permits V_{OL} tests.

A. C. CHARACTERISTICS With Standard Load

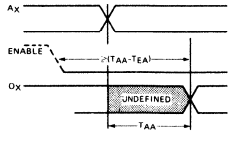
PARAMETER	SYMBOL	FIGURE	5305/5306 5.00 V, 25°C		6305/6306 5.00 V, 25°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	1	10	70	10	70
Enable Access Time	T_{EA}	2	5	35	5	35
Enable Recovery Time	T_{ER}	2	5	35	5	35
5306/6306 ONLY						
Chip Enable to Low Impedance Delay	T_{ON}		5		5	
Chip Enable to High Impedance Delay	T_{OFF}			30		30

STANDARD TEST LOAD



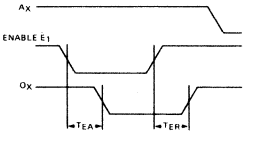
Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 15 mA and 30 pF as given in std. load

Fig. 1
ADDRESS ACCESS TIME



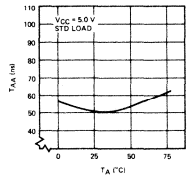
A_X = Any Address
O_X = Any Output

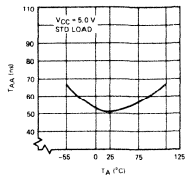
Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME

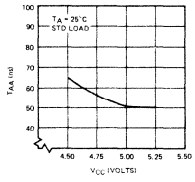


ELECTRICAL PARAMETERS

CURVES OF TYPICAL DEVICES







Note: The T_{EA} parameter typically varies from 21 to 33 ns for any device type over the voltage and temperature range of 5 V ±10%, −55 to 125°C.

PULLUP RESISTOR SELECTION FOR 5305 AND 6305

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 16 mA for the 6305
10 mA for the 5305
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four 6305 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V.

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 16 mA

$$R_L(\text{max}) = \frac{V_{CC}-2.40\ V}{M(100\ \mu A)+N(I_R)} \qquad R_L(\text{max}) = \frac{5.0-2.4\ V}{4\ (100\ \mu A)+3\ (40\ \mu A)} = 5000 \text{ ohms}$$

$$R_L(\text{min}) = \frac{V_{CC}-0.45\ V}{I_{OL}-N(I_F)} \qquad R_L(\text{min}) = \frac{5.0-0.45\ V}{16\ mA-3(1.6\ mA)} = 406 \text{ ohms}$$

THREE-STATE OUTPUT — See Figures A and B

FIGURE A
THREE-STATE OUTPUT

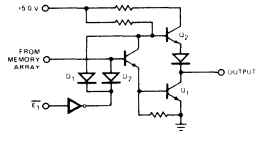
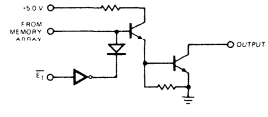


FIGURE B
OPEN COLLECTOR OUTPUT



The three-state output of the 5306/6306 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip enable is low D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment, up to 21 outputs of the 6306 or 10 outputs of the 5306 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

MEMORY OPERATION

The memory is addressed with inputs A_0 through A_8 which select one of 512 words. A four bit parallel readout is available for each word on outputs O_1 to O_4. To enable the outputs for a readout, enable $\overline{E}_1$ must be low. If the enable is high, the outputs are held off permitting wire"OR"ing of three-state or open collector outputs of several packages. The use of the enables permits expansion to greater than 512 words.

PROGRAMMING INSTRUCTIONS

1) DEVICE DESCRIPTION

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. There are 2048 fusible links on the chip. Programming equipment can be obtained from Monolithic Memories Inc.

2) PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_8, a V_{CC} of 5.50 V is applied or left applied, and the program pin (Enable $\overline{E}_1$) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

3) TIMING

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate.
The programming pulse applied to the output pin must have 10 microseconds or slower rise time to avoid capacitively coupling the output signal into the base of the output transistor, causing it to turn on and go into avalanche breakdown. This coupling would occur during the low to high transition of the output pin's programming pulse through the output transistors' collector to base capacitance. Similar consideration limit the rise time of the program pin. Fall times are not critical.

4) VERIFICATION

After programming a device, it can be checked for a low output by taking the enable low. Since we are checking for a programmed high resistance fusible link and must guarantee operation at minimum voltage, maximum sink current, and cold temperature, the device must be required to sink 12 mA at 4.20 V V_{CC} at room temperature to guarantee a fully programmed link.

5) BOARD PROGRAMMING

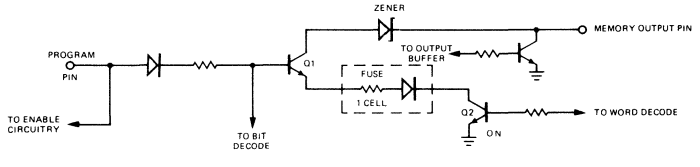
Units may be programmed at the board level by bringing the program pin of each package to the card connector. To program a particular package "A", the program pin of package A and one output of package A, which may or may not be "OR" tied to other packages, are taken to the required programming voltage. An alternate procedure is to tie the enable and outputs together as required by the system function and only apply V_{CC} to the device to be programmed. The number of units soldered on a board should be consistent with expected programming yields to avoid rework.

6) UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. **UNITS RETURNED TO MMI AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULDN'T BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

OPERATION

PROGRAMMING EQUIVALENT CIRCUIT FOR ONE MEMORY OUTPUT



The word decode circuitry selects transistor Q_2 to be turned on, and the bit decode circuitry allows the base of Q_1 to rise. 2047 other fuses are half selected or not selected. The program pin supplies base drive to Q_1 and the output pin supplies collector current to Q_1 so that Q_1's emitter can deliver the required current to open the fusible link.

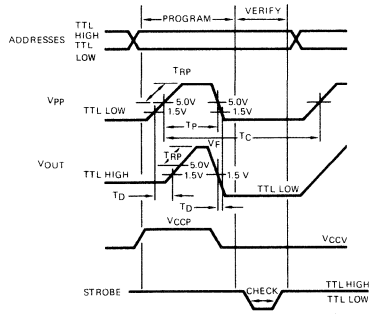
FIGURE 3

PROGRAMMING INFORMATION

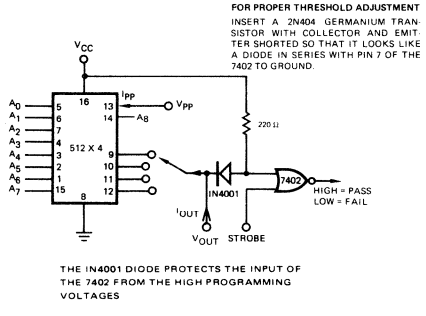
PROGRAMMING PARAMETERS – Do Not Test These Limits or You May Program The Device.

SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS MIN.	LIMITS TYPICAL OR OPTIMUM	LIMITS MAX.	UNITS
I_{pp}	Current into Program Pin During Programming, Before and After Fuse Has Blown	V_{CC} = 5.50 V V_{out} = 5.0 V to 25 V V_{pp} = 4.50 V		0		mA
		V_{pp} = 29 V		150		mA
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{pp} = 29 V, V_{CC} = 5.50 V V_{out} = 9.0 V		0.1		mA
		V_{out} = V		16		mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{pp} = 29 V, V_{out} = V V_{CC} = 5.50 V		10		mA
T_{RP}	Rise Time of Program Pulse Applied to the Data out or Program Pin From 5 V to 20 V		10.0	20±10	100	μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
V_{CCV}	V_{CC} Required During Verification	Both Chip Enables Low	4.10	4.20	4.30	V
I_{OLV}	Output Current Required to Guarantee a Fully Programmed Link	T_A = 25°C, V_{CC} = 4.20 V	12			mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	$\frac{T_P}{T_C}$			25	%
V_{pp}	Required Programming Voltage on Program Pin		28		34	V
V_{out}	Required Programming Voltage on the Output Pin		20		26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{pp} = 33 V V_{out} = 25 V V_{CC} = 5.50 V	240			mA
T_p	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		0.040		300	ms
T_D	Required Time Delay Between Disabling the Memory Output and Application or Removal of the Output Programming Pulse (see Item 4, page 4)	Measure at 1.5 V Levels	100			ns

TIMING



SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY



THE IN4001 DIODE PROTECTS THE INPUT OF THE 7402 FROM THE HIGH PROGRAMMING VOLTAGES

FIGURE 4

PROGRAMMING INFORMATION

PROGRAMMING SPEED

Most fuses will blow on the rise time of the pulse and in less than 10 microseconds. Some fuses however, will require the thermal energy required by higher programming voltages and wider programming pulse widths (up to 200 milliseconds) to open.

In simple programming schemes where the programming time is not critical the wider pulses can be used exclusively. In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to give maximum thruput (less than 3 seconds per device on the average) and programming yield. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	DURATION	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 4	40 μs	29 V	20 V
5 to 8	40 μs	33 V	25 V
9 to 12	20 ms	33 V	25 V
13 to 16	200 ms	33 V	25 V

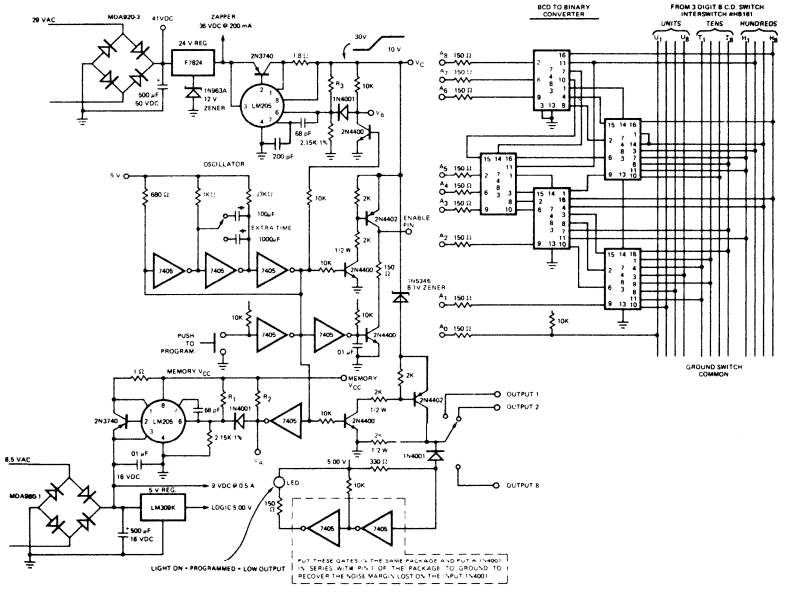
PROGRAMMER DESCRIPTION

Figure 5 below shows the circuitry required to build a simple manual programmer. The operator with this programmer dials in the memory address to be programmed on a three digit thumbwheel switch and selects the output to be programmed or readout on a 4 position rotary switch. Pushing the program button will open the nichrome link at the selected address. When the program button is released the memory data is displayed on an LED.

OPERATION

Five 7483's are used to convert from BCD to binary addresses. An LM205 is used to control the device V_{CC} and vary it from 4.20 to 5.50 V depending upon whether V_A is high or low. V_A and V_B are controlled by the oscillator which is turned on when the program button is pushed. V_A and V_B vary the device V_{CC} and programming voltage by changing the resistor divider values on the LM205 which set the output voltage. Two oscillator speeds can be selected by a two position switch.

MANUAL PROGRAMMER



NOTES:

1. Adjust R_1 and R_2 so that the memory V_{CC} is 4.150 to 4.250 V quiescent and 5.450 to 5.550 V when the program button is pushed. $R_1 \approx 5K$. $R_2 \approx 15K$.
2. Adjust R_3 for 30 to 31 V on V_C when the program button is pushed. $V_C \approx \frac{R_3\,(K\Omega)}{2.15k}\,(1.7\ V)$ SO $R_3 \approx 37K$
3. Use Thermalloy heat sink #6166B on both 2N3740 transistors.

REQUIRED INFORMATION FOR MMI TO PROGRAM TO YOUR TRUTH TABLE

TRUTH TABLES

MMI can program devices at our facility from MMI truth table forms (available on request). For customers desiring to make their own forms, an example is shown below:

		OUTPUTS			
WORD	PIN →	9	10	11	12
NUMBER		O_4	O_3	O_2	O_1
0		H	H	H	L
1		L	H	L	H
.		.	.	.	.
.		.	.	.	.
511		L	H	H	H

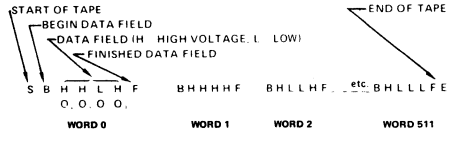
Note: A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pins, so for example, word 255 = HHHHHHHH.

PAPER TAPE FORMAT

Truth tables can also be sent to MMI in an ASCII tape format. Information can be sent to us by air mail or TWX 910-339-9224. The tape reading equipment at MMI only recognizes ASCII characters S, B, H, L, F and E and interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to word 511.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is O_4, O_3, O_2, O_1, not O_1, O_2, O_3, O_4.

A typical list of charaters and their machine interpretations are shown below:



The required heading information at the beginning of the tape is as follows:

CUSTOMERS NAME AND PHONE _____ TRUTH TABLE NUMBER _____

CUSTOMERS TWX NUMBER _____ NUMBER OF TRUTH TABLES _____

PURCHASE ORDER NUMBER _____ TOTAL NUMBER OF PARTS _____

MMI PART NUMBER _____ NUMBER OF PARTS OF EACH TRUTH TABLE _____

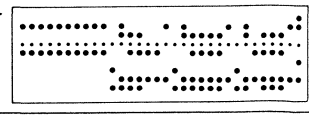
CUSTOMER SYMBOLIZED PART NUMBER _____ 25 BELL OR RUBOUT CHARACTERS _____

An example is shown below:

BLARNEY ELECTRONICS 408-735-8104
TWX 911-338-9225
P0142
6305
0431
12
1
3
3

SBLLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF BLLLLF
BLLLLF BLHLHF BLLHHF BHHHLF BHHLLF BLLHHF BHHLLF BLLHHF BLHLHF

8 LEVEL TWX

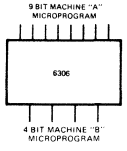


APPLICATIONS

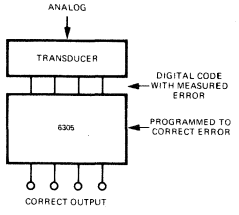
GENERAL

The P. ROM was designed for situations which require a fast turnaround on bit patterns. The device permits patterns to be changed in the field in minutes. The pin and performance compatibility with the mask programmable 5205/6205 permits fast prototyping and the economic advantages of mask made ROM. The interchangeability and side by side operation of the ROM and P. ROM offers an effective means of customizing a small portion of a machine, or permitting engineering changes, or eliminating field stocking of mask programmable ROMs.

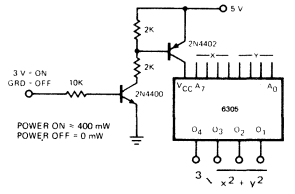
EMULATION



TRANSDUCER ERROR CORRECTION

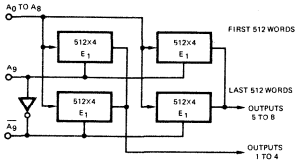


LOW POWER FUNCTION GENERATION

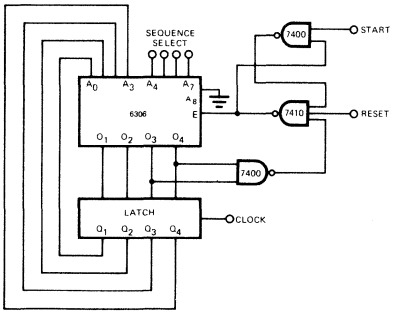


MEMORY EXPANSION 1024 X 8 SYSTEM

The highest order address (A_9) is used in conjunction with the chip enables to select either the first 512 words (when A_9 is low) or the last 512 words (when A_9 is high). The corresponding outputs of the packages in the same column are OR tied for the 8 bit readout required.



SEQUENCE GENERATOR



ADDRESS	A_7	A_6	A_5	A_4	SEQUENCE NO.
0 TO 15	L	L	L	L	1) SERVICE TELETYPE
16 TO 31	L	L	L	H	2) SERVICE PRINTER
.		.			.
.		.			.
.		.			.
239 TO 255	H	H	H	H	16) SERVICE TAPE UNIT

The enable is used to define a known starting point since when it is high the memory outputs are high regardless of the programmed code.

RANDOM LOGIC REPLACEMENT

$F1 = (\bar{A}BCD + A\bar{B}CD + ABC\bar{D}) \cdot \bar{E}\bar{F}\bar{G}\bar{H}$

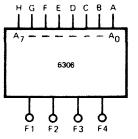
INTERPRETATION:

F1 is high if address 14, 13, 11 or 7 is selected

$F2 = (\bar{A}BCD + BC\bar{D}) \cdot \bar{E}\bar{F}\bar{G}\bar{H}$

INTERPRETATION:

F2 is high if address 12, 7 or 6 is selected



F3 $E \cdot F \cdot G \cdot H$ PLUS 1

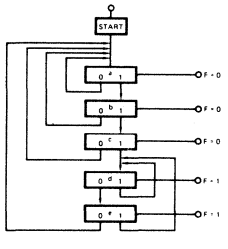
F4 $E \cdot F \cdot \bar{G} \cdot H$ MINUS 1

COMBINATION LOCK OR SEQUENCE DETECTOR

Design a circuit which after initially set to zero, will go to 1 if 3 or more consecutive 1's appear on the input. It should remain at logical 1 until two consecutive logical 0's appear.

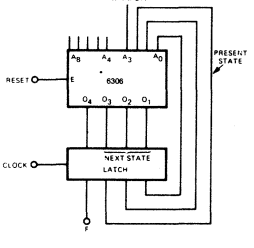
Assign machine states a thru e to the five possible states of the system and call the output F and the input X.

FLOWCHART



STATE TABLE

PRESENT STATE	NEXT STATE X = 0	NEXT STATE X = 1	OUTPUT F OF PRESENT STATE
a	a	b	0
b	a	c	0
c	a	d	0
d	e	d	1
e	a	d	1



256 BIT BIPOLAR (32x8) ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

5330/6330
5331/6331

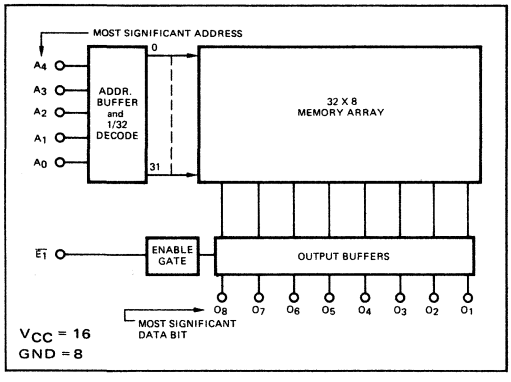
Monolithic Memories
INCORPORATED

PRODUCT FEATURES:

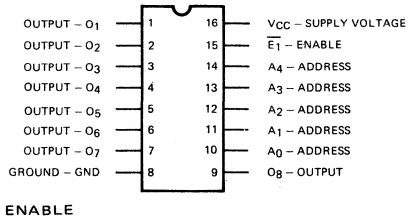
- Field Programmable with Simple Programming Procedure
- Pin Compatible with Mask Programmable 5230/6230 5231/6231
- Fast Programming Time — Average of 5 ms/Bit
- Standard Packaging — 16 Pin DIP
- Fully Decoded — On Chip Address Decoding
- DTL and TTL Compatible
- Three-State or Open Collector Outputs
- Special On Chip Circuitry Permits V_{OL} Testing Before Programming

	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
6330		X		X
6331		X	X	
5330	X			X
5331	X		X	

BLOCK DIAGRAM: 32 WORDS X 8 BITS MEMORY



PIN CONFIGURATION



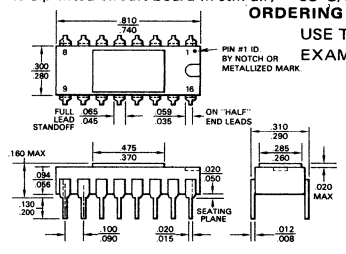
LOW = ENABLE

PACKAGE OUTLINE

16 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/watt

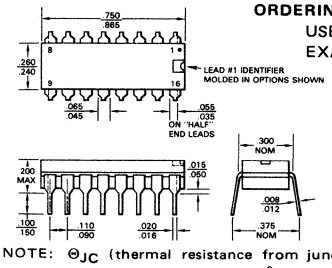
ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6330D



16 Pin Ceramic (CERDIP)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 75°C/watt

ORDERING INFORMATION
USE THE SUFFIX J
EXAMPLE 6330J



NOTE: Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt for both packages.

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

MARCH 1974

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V	Pin 14 Voltage During Vol Tests	13 V
Input Voltage	−1.0 to 5.5 V	Output Voltage During Programming	27 V
Output Current	100 mA	Programming Duty Cycle	30% MAX.
Input Current	−20 to 5 mA	Stresses above or extended time at Absolute Maximum Ratings	
Storage Temperature	−65 to +150°C	may cause permanent damage or affect device reliability.	

D.C. CHARACTERISTICS:

Unless otherwise indicated, all limits for the 6330/6331 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5330/5331 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C

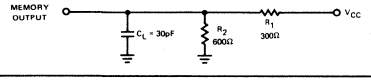
PARAMETER		CONDITIONS	5330/5331			6330/6331			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All inputs	V_{CC} = Max, V_F = 0.45 V		−1.0	−1.6		−1.0	−1.6	mA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			40			40	µA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 10 mA		0.35	0.45				V
	See Note 2 Below	V_{CC} = Min, I_{OL} = 16 mA					0.35	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, Inputs GRD, All Outputs Open — 5330/6330		80	100		80	100	mA
		V_{CC} = 5.0 V, Inputs GRD, All Outputs Open — 5331/6331		90	125		90	125	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current 5330/6330 Only	V_{CC} = Max, V_{CEX} = 2.40 V			100		100		µA
		V_{CC} = Max = V_{CEX}			1			1	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5 mA		−1.0	−1.5		−1.0	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF
THREE STATE PARAMETERS — 5331/6331 ONLY									
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5.0 V	−20	−50	−90	−20	−50	−90	mA
I_{HZ}	Output Leakage High Impedance State	V_{CC} = Max, V_O = 0.45 V to 2.4 V Chip Disabled			±100			±100	µA
V_{OH}	Output Voltage "High"	I_O = −2.0 mA for the 6331 I_O = −900 µA for the 5331	2.4	3.2		2.4	3.2		V

1. Typical values are measured at 5.0 V and 25°C.
2. Unprogrammed P.ROMS will have all outputs high. V_{OL} can be tested by enabling the device and taking pin 14 to 10 V (less than 10 mA must be supplied) and pin 13 to a voltage between 2.4 V and 5.0 V. This procedure turns on all 8 outputs and permits V_{OL} tests.

A.C. CHARACTERISTICS With Standard Load

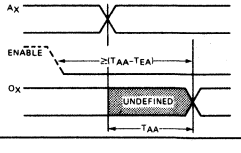
PARAMETER	SYMBOL	FIGURE	5330/5331 5.0 V, 25°C		6330/6331 5.0 V, 25°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	1	10	50	10	50
Enable Access Time	T_{EA}	2	5	30	5	30
Enable Recovery Time	T_{ER}	2	5	30	5	30
5331/6331 ONLY						
Chip Enable to Low Impedance Delay	T_{ON}		5		5	
Chip Enable to High Impedance Delay	T_{OFF}			30		30

STANDARD TEST LOAD



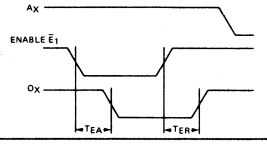
Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 15 mA and 30 pF as given in std. load

Fig. 1
ADDRESS ACCESS TIME

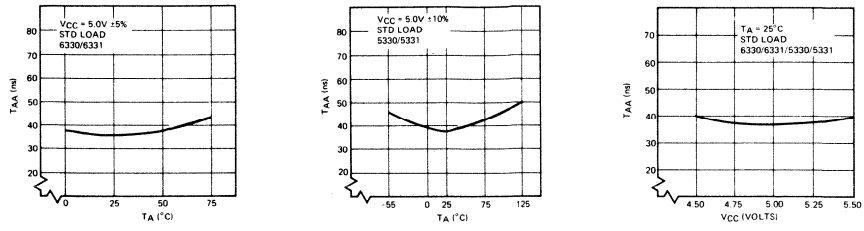


A_X = Any Address
O_X = Any Output

Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



CURVES OF TYPICAL DEVICES



Note: The T_{EA} parameter typically varies from 21 to 33 ns for any device type over voltage and temperature for 5 V ±10%, −55 to 125°C.

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 16 mA for the 6330/6331
10 mA for the 5330/5331
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four 6330 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 16 mA

$$R_L(\text{max}) = \frac{V_{CC} - 2.40\ V}{M(100\ \mu A) + N(I_R)} \qquad R_L(\text{max}) = \frac{5.0 - 2.4\ V}{4(100\ \mu A) + 3(40\ \mu A)} = 5000 \text{ ohms}$$

$$R_L(\text{min}) = \frac{V_{CC} - 0.45\ V}{I_{OL} - N(I_F)} \qquad R_L(\text{min}) = \frac{5.0 - 0.45\ V}{16\ mA - 3(1.6\ mA)} = 406 \text{ ohms}$$

THREE-STATE OUTPUT — SEE FIGURES A AND B

FIGURE A
THREE-STATE OUTPUT

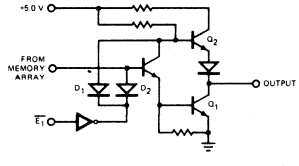
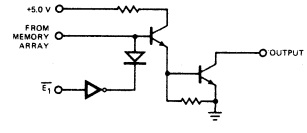


FIGURE B
OPEN COLLECTOR OUTPUT



The three-state output of the 5331/6331 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment, up to 21 memory outputs of the 6331 or 10 outputs of the 5331 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

PROGRAMMING INSTRUCTIONS

1) DEVICE DESCRIPTION

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. There are 256 fusible links on the chip. Programming equipment can be obtained from Monolithic Memories Inc.

2) PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_4, a V_{CC} of 5.50 V is applied or left applied, the enable is disabled by applying a TTL high level, (2.40 to 5.50 V), and the output to be programmed is taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Repeated programming attempts will not damage the device.

3) TIMING

The programming procedure involves the use of the enable ($\overline{E_1}$) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the enable's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate.

The programming pulse applied to the output pin must have 10 microseconds or slower rise time to avoid capacitively coupling the output signal into the base of the output transistor, causing it to turn on and go into avalanche breakdown. This coupling would occur during the low to high transition of the output pin's programming pulse through the output transistors' collector to base capacitance. Fall times are not critical.

4) VERIFICATION

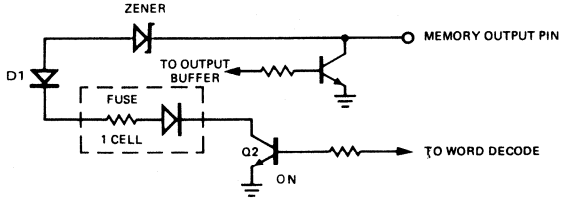
After programming a device, we can check whether the output is low by taking the enable low. Since we are checking for a programmed high resistance fusible link and must guarantee operation at minimum voltage, maximum sink current and cold temperature, the device must be required to sink 12 mA at 4.20 V V_{CC} at room temperature to guarantee a fully programmed link.

5) UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. **UNITS RETURNED TO MMI AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULDN'T BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

OPERATION

PROGRAMMING EQUIVALENT CIRCUIT FOR ONE MEMORY OUTPUT



The word decode circuitry selects transistor Q_2 to be turned on. 255 other fuses are half selected or not selected. The output pin supplies the required current through D1 to open the fusible link.

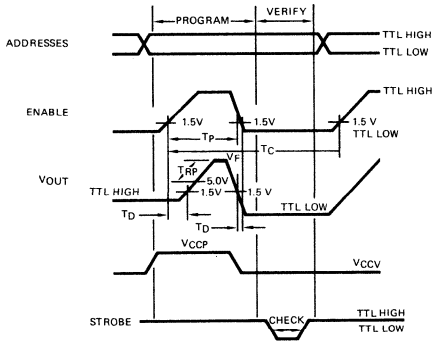
FIGURE 3

PROGRAMMING INFORMATION

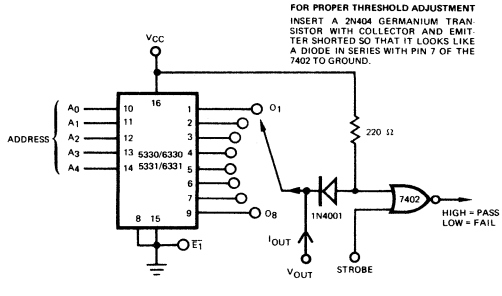
PROGRAMMING PARAMETERS – DO NOT TEST THESE LIMITS OR YOU MAY PROGRAM THE DEVICE.

SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS MIN.	LIMITS TYPICAL OR OPTIMUM	LIMITS MAX.	UNITS
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{CC} = 5.0 V V_{out} = 9.0 V V_{out} = 25 V		0.1 35		mA mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{out} = 20 V V_{CC} = 5.50 V		3		mA
T_{RP}	Rise Time of Program Pulse Applied to the Data Out From 5.0 V to 20 V		10	20±10	100	μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
V_{CCV}	V_{CC} Required During Verification	Chip Enable Low	4.10	4.20	4.30	V
I_{OLV}	Output Current Required to Guarantee a Fully Programmed Link	T_A = 25°C, V_{CC} = 4.20 V	12			mA
MDC	Maximum Duty Cycle During Automatic Programming of Enable and Output Pin	$\frac{T_P}{T_C}$			25	%
V_{out}	Required Programming Voltage on the Output Pin		20		26	V
I_L	Required Current Limit of the Power Supply Feeding the Output During Programming	V_{out} = 25 V V_{CC} = 5.50 V	150			mA
T_p	Required Coincidence Among the Enable, Output, Address and V_{CC} for Programming		0.040		300	ms
T_D	Required Time Delay Between Disabling the Memory Output and Application or Removal of the Output Programming Pulse (see Item 4, page 4)	Measure at 1.5 V Levels	100			ns

TIMING



SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY



THE 1N4001 DIODE PROTECTS THE INPUT OF THE 7402 FROM THE HIGH PROGRAMMING VOLTAGES

FIGURE 4

PROGRAMMING INFORMATION

PROGRAMMING SPEED

Most fuses will blow on the rise time of the pulse and in less than 10 microseconds. Some fuses however, will require the thermal energy required by higher programming voltages and wider programming pulse widths (up to 200 milliseconds) to open.

In simple programming schemes where the programming time is not critical the wider pulses can be used exclusively. In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to give maximum thruput (less than 3 seconds per device on the average) and programming yield. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	DURATION	OUTPUT VOLTAGE
1 to 4	40 μs	20 V
5 to 8	40 μs	25 V
9 to 12	20 ms	25 V
13 to 16	200 ms	25 V

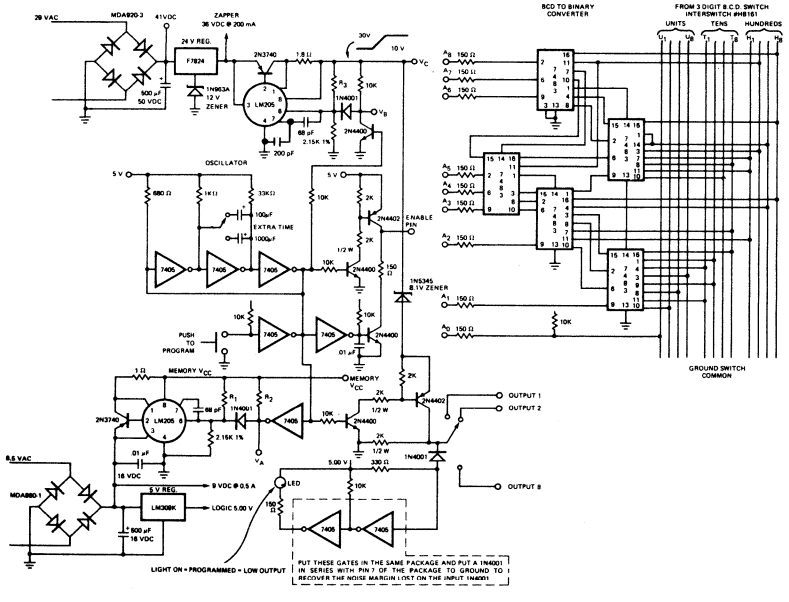
PROGRAMMER DESCRIPTION

Figure 5 below shows the circuitry required to build a simple manual programmer. The operator with this programmer dials in the memory address to be programmed on a three digit thumbwheel switch and selects the output to be programmed or readout on an 8 position rotary switch. Pushing the program button will open the nichrome link at the selected address. When the program button is released the memory data is displayed on an LED.

OPERATION

Five 7483's are used to convert from BCD to binary addresses. An LM205 is used to control the device V_{CC} and vary it from 4.20 to 5.50 V depending upon whether V_A is high or low. V_A and V_B are controlled by the oscillator which is turned on when the program button is pushed. V_A and V_B vary the device V_{CC} and programming voltage by changing the resistor divider values on the LM205 which set the output voltage. Two oscillator speeds can be selected by a two position switch.

MANUAL PROGRAMMER



NOTE: A_5 THRU A_8 ARE NOT USED ON THE 32X8.

NOTES:

1. Adjust R_1 and R_2 so that the memory V_{CC} is 4.150 to 4.250 V quiescent and 5.450 to 5.550 V when the program button is pushed. $R_1 \approx 5K$, $R_2 \approx 15K$.
2. Adjust R_3 for 31 to 33 V on V_C when the program button is pushed. $V_C \approx \frac{R_3\ (k\Omega)}{2.15\ k}\ (1.7\ V)$ so $R_3 \approx 41K$.
3. Use Thermalloy heat sink #6166B on both 2N3740 transistors.

REQUIRED INFORMATION FOR MMI TO PROGRAM TO YOUR TRUTH TABLE

TRUTH TABLES

MMI can program devices at our facility from MMI truth table forms (available on request). For customers desiring to make their own forms, an example is shown below:

		OUTPUTS							
WORD	PIN →	9	7	6	5	4	3	2	1
NUMBER		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0		H	H	H	L	H	L	H	L
1		L	H	L	H	L	L	H	H
.		.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.
31		L	H	H	H	H	L	H	L

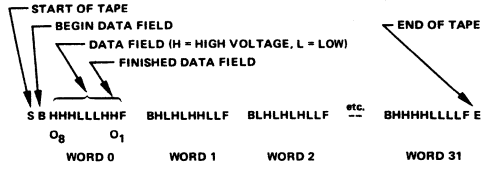
Note: A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pins, so,for example, word 31 = HHHHH.

PAPER TAPE FORMAT

Truth tables can also be sent to MMI in an ASCII tape format. Information can be sent to us by air mail or TWX 910-339-9224. The tape reading equipment at MMI only recognizes ASCII characters S, B, H, L, F and E and interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to word 31.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is 0_8 to 0_1, not 0_1 to 0_8.

A typical list of characters and their machine interpretations are shown below:



The required heading information at the beginning of the tape is as follows:

CUSTOMERS NAME AND PHONE _____ TRUTH TABLE NUMBER _____

CUSTOMERS TWX NUMBER _____ NUMBER OF TRUTH TABLES _____

PURCHASE ORDER NUMBER _____ TOTAL NUMBER OF PARTS _____

MMI PART NUMBER _____ NUMBER OF PARTS OF EACH TRUTH TABLE _____

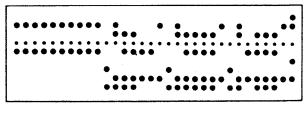
CUSTOMER SYMBOLIZED PART NUMBER _____ 25 BELL OR RUBOUT CHARACTERS _____

An example is shown below for a 256 x 4 Prom (6300)

BLARNEY ELECTRONICS 408-735-8104
TWX 911-338-9225
P0142
6300
0431
12
1
3
3

SBLLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF BLLLLF
BLLLLF BLHLHF BLLHHF BHHHLF BHHLLF BLLHHF BHHLLF BLLHHF BLHLHF

8 level TWX

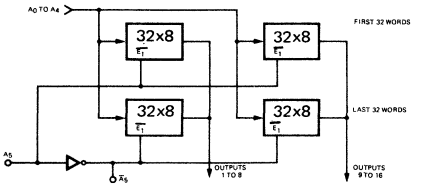


APPLICATION INFORMATION

The P.ROM was designed for situations which require a fast turnaround on bit patterns. The device permits patterns to be changed in the field in minutes. The pin and performance compatibility with the mask programmable 256 x 4 ROM permits fast prototyping and the economic advantages of mask made ROM. The interchangeability and side by side operation of the ROM and P.ROM offers an effective means of customizing a small portion of a machine, or permitting engineering changes, or eliminating field stocking of mask programmable ROMs.

MEMORY EXPANSION 64 X 16 SYSTEM

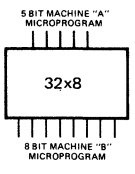
The highest order address (A_5) is used in conjunction with the chip enable to select either the first 32 words (when A_5 is low) or the last 32 words (when A_5 is high). The corresponding outputs of the packages in the same column are OR tied for the 16 bit readout required.



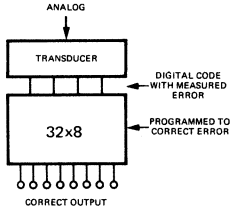
GENERAL

The 5330/6330/5331/6331 was designed for situations which require a fast turnaround on bit patterns. The device permits patterns to be changed in the field in minutes. The pin and performance compatibility with the mask programmable 5230/6230/5231/6231 permits fast prototyping and the economic advantages of mask made ROM. The interchangeability and side by side operation of the ROM and PROM offers an effective means of customizing a small portion of a machine, or permitting engineering changes, or eliminating field stocking of mask programmable ROMs.

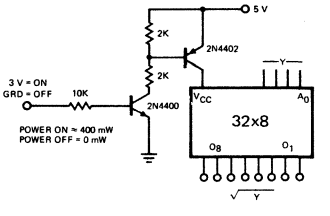
EMULATION

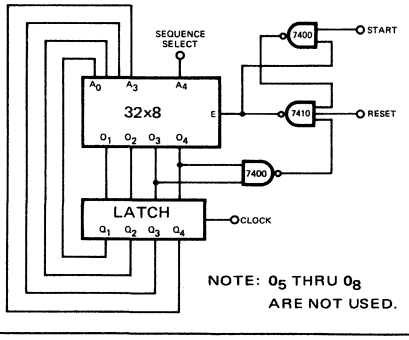


TRANSDUCER ERROR CORRECTION



LOW POWER FUNCTION GENERATION





NOTE: O_5 THRU O_8 ARE NOT USED.

ADDRESS	A_4	SEQUENCE NO.
0 TO 15	L	1) SERVICE TELETYPE
16 TO 31	H	2) SERVICE PRINTER

The enable is used to define a known starting point since when it is high the memory outputs are high regardless of the programmed code.

RANDOM LOGIC REPLACEMENT

$F1 = (\bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D}).\ \bar{E}$

INTERPRETATION:

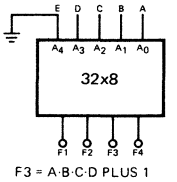
F1 is high if address 14, 13, 11 or 7 is selected

$F2 = (\bar{A}BCD + BC\bar{D}).\bar{E}$

INTERPRETATION:

F2 is high if address 12, 14 or 15 is selected

NOTE: ONLY 16 WORDS AND 4 OUTPUTS OF THE 32 X 8 ARE USED



F3 = A·B·C·D PLUS 1
F4 = A·B·C·D MINUS 1

MEMORY OPERATION

The memory is addressed with inputs A_0 through A_4 which select one of 32 words. An eight bit parallel readout is available for each word on outputs O_1 to O_8. To enable the outputs for a readout, enable $\overline{E_1}$ must be low. If the enable is high the outputs are held off permitting wire "OR"ing of the three-state outputs of several packages. The use of the enable permits expansion to greater than 32 words.

4096 BIT (512 x 8) AND 2048 BIT (256 x8) BIPOLAR ELECTRICALLY PROGRAMMABLE READ ONLY MEMORIES

5340/6340
5335/6335

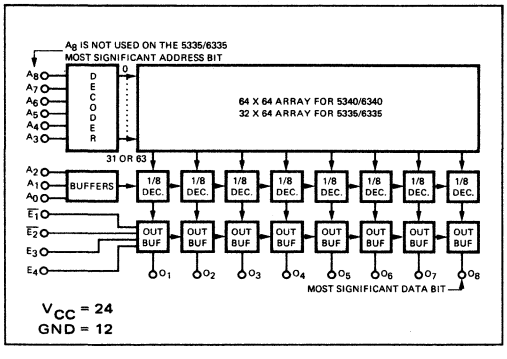
Monolithic Memories
INCORPORATED

PRODUCT FEATURES:

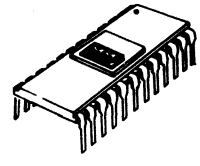
- Field Programmable with Simple Programming Procedure
- Pin and Performance Compatible with Mask Programmable 5240/6240, 5235/6235
- Fast Programming Time — Typically 5 ms/Bit
- Standard Packaging — 24 Pin DIP
- Fully Decoded — On Chip Address Decoding
- DTL and TTL Compatible
- Open Collector Outputs
- Special On Chip Circuitry Permits V_{OL} Testing Before Programming

	MILITARY	COMMERCIAL	512X8	256X8
6340		X	X	
5340	X		X	
6335		X		X
5335	X			X

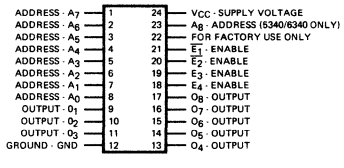
BLOCK DIAGRAM:



PACKAGE OUTLINE



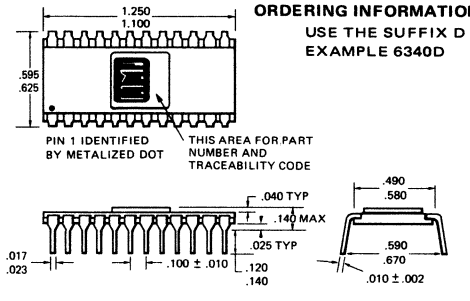
PIN CONFIGURATION



Note: 1) A_8 is not Connected on the 5335/6335
2) Pin 22 Must Be Left Open
3) The Chip is Enabled when $\overline{E_1}$ and $\overline{E_2}$ are Low and E_3 and E_4 are High.

PACKAGE OUTLINE

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 48°C/watt



ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6340D

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt.

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

NOVEMBER 1973

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V	Pin 5 Voltage During V_{OL} Tests	14 V
Input Voltage	−1.0 to 5.5 V	Output Voltage During Programming	27 V
Output Current	100 mA	Programming Duty Cycle	25% MAX.
Input Current	−20 to 5 mA	Stresses above or extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.	
Storage Temperature	−65 to +150°C		

D.C. CHARACTERISTICS:

Unless otherwise indicated, all limits for the 6340/6335 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5340/5335 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C

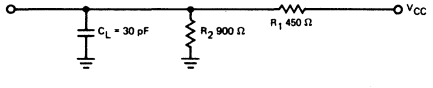
PARAMETER		CONDITIONS	5340/5335			6340/6335			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All inputs	V_{CC} = Max, V_F = 0.45 V			−250			−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			40			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 8 mA		0.35	0.50				V
	See Note 2 Below	V_{CC} = Min, I_{OL} = 10 mA					0.35	0.50	V
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Open, All Outputs Open		80	140		80	140	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.40 V			100			100	μA
	High Stored or Disabled	V_{CC} = Max = V_{CEX}			1			1	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5 mA		1.0	−1.5		−1.0	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF

1. Typical values are measured at 5.0 V and 25°C.
2. Unprogrammed P.ROMS will have all outputs high. V_{OL} can be tested by enabling the device and taking pin 5 to 12 V (less than 10 mA must be supplied). This procedure turns on all outputs and permits V_{OL} tests.

A.C. CHARACTERISTICS WITH STANDARD LOAD

PARAMETER	SYMBOL	FIGURE	5340/5335 5.00 V, 25°C		6340/6335 5.00 V, 25°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	1	20	90	20	90
Enable Access Time	T_{EA}	2	10	40	10	40
Enable Recovery Time	T_{ER}	2	10	40	10	40

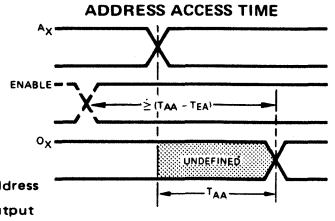
STANDARD TEST LOAD



Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 10 mA and 30 pF as given in std. load

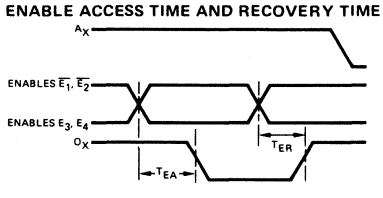
TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

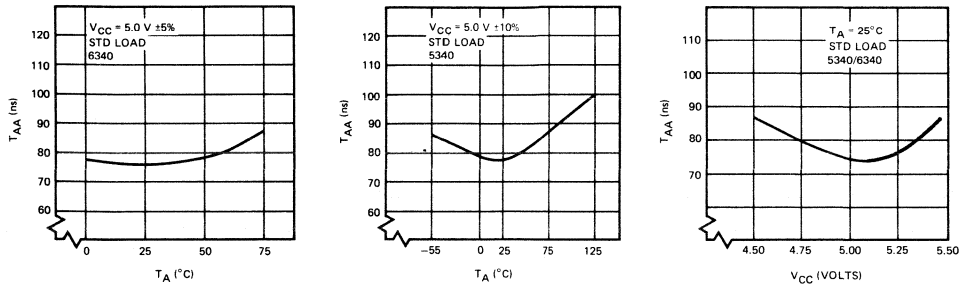


A_X = Any Address
O_X = Any Output

Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



CURVES OF TYPICAL DEVICES



Note: The T_{EA} parameter typically varies from 20 to 37 ns for any device type over voltage and temperature for 5 V ±10%, −55 to 125°C.

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 10 mA for the 6340
8 mA for the 5340
I_F = The maximum input load current of the TTL family at 0.50 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four **6340** memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 10 mA

$$R_L(\text{max}) = \frac{V_{CC} - 2.40\ V}{M(100\ \mu A) + N(I_R)} \qquad R_L(\text{max}) = \frac{5.0 - 2.4\ V}{4(100\ \mu A) + 3(40\ \mu A)} = 5000 \text{ ohms}$$

$$R_L(\text{min}) = \frac{V_{CC} - 0.50\ V}{I_{OL} - N(I_F)} \qquad R_L(\text{min}) = \frac{5.0 - 0.50\ V}{10\ mA - 3(1.6\ mA)} = 865 \text{ ohms}$$

PROGRAMMING INSTRUCTIONS

1) DEVICE DESCRIPTION

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. Programming equipment can be obtained from Monolithic Memories Inc.

2) PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_8 (A_7 on the 5335/6335), a V_{CC} of 5.50 V is applied or left applied, the chip is disabled by applying the appropriate TTL levels to the enables, and the output to be programmed is taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Repeated programming attempts will not damage the device.

3) TIMING

The programming procedure involves the use of the enables and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the enable's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate.

The programming pulse applied to the output pin must have 10 microseconds or slower rise time to avoid capacitively coupling the output signal into the base of the output transistor, causing it to turn on and go into avalanche breakdown. This coupling would occur during the low to high transition of the output pin's programming pulse through the output transistors' collector to base capacitance. Fall times are not critical.

4) VERIFICATION

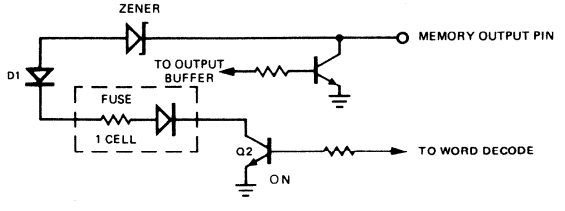
After programming a device, we can check whether the output is low by taking the enable low. Since we are checking for a programmed high resistance fusible link and must guarantee operation at minimum voltage, maximum sink current and cold temperature, the device must be required to sink 12 mA at 4.20 V V_{CC} at room temperature to guarantee a fully programmed link.

5) UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. UNITS RETURNED TO MMI AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULDN'T BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.

OPERATION

PROGRAMMING EQUIVALENT CIRCUIT FOR ONE MEMORY OUTPUT



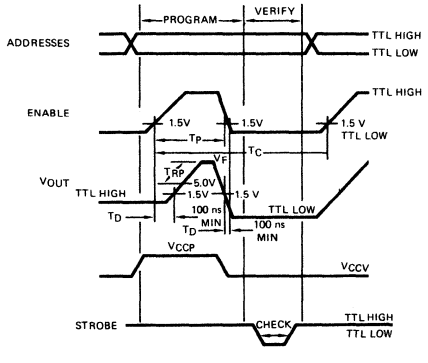
The word decode circuitry selects transistor Q_2 to be turned on. All other fuses are half selected or not selected. The output pin supplies the required current through D1 to open the fusible link.

FIGURE 3

PROGRAMMING PARAMETERS – DO NOT TEST THESE LIMITS OR YOU MAY PROGRAM THE DEVICE.

SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS MIN.	LIMITS TYPICAL OR OPTIMUM	LIMITS MAX.	UNITS
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{CC} = 5.0 V V_{out} = 9.0 V V_{out} = 25 V		3 25		mA mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{out} = 25 V V_{CC} = 5.50 V		8		mA
T_{RP}	Rise Time of Program Pulse Applied to the Data Out From 5.0 V to 20 V		10	20±10	100	μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
V_{CCV}	V_{CC} Required During Verification	Chip Enable Low	4.10	4.20	4.30	V
I_{OLV}	Output Current Required to Guarantee a Fully Programmed Link	T_A = 25°C, V_{CC} = 4.20 V	12			mA
MDC	Maximum Duty Cycle During Automatic Programming of Enable and Output Pin	$\frac{T_P}{T_C}$			25	%
V_{out}	Required Programming Voltage on the Output Pin		20		25	V
I_L	Required Current Limit of the Power Supply Feeding the Output During Programming	V_{out} = 25 V V_{CC} = 5.50 V	150			mA
T_p	Required Coincidence Among the Enable, Output, Address and V_{CC} for Programming		0.040		300	ms
T_D	Required Time Delay Between Disabling the Memory Output and Application or Removal of the Output Programming Pulse (see Item 4, page 4)	Measure at 1.5 V Levels	100			ns

TIMING



SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY

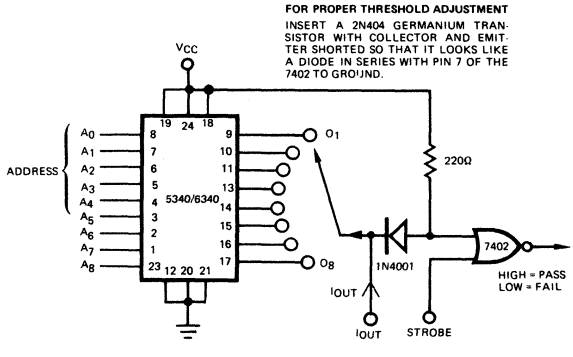


FIGURE 4

PROGRAMMING INFORMATION

PROGRAMMING SPEED

Most fuses will blow on the rise time of the pulse width and in less than 10 microseconds. Some fuses however, will require the thermal energy required by higher programming voltages and wider programming pulse widths (up to 200 milliseconds) to open.

In simple programming schemes where the programming time is not critical the wider pulses can be used exclusively. In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to give maximum thruput (less than 3 seconds per device on the average) and programming yield. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	DURATION	OUTPUT VOLTAGE
1 to 4	40 μs	20 V
5 to 8	40 μs	25 V
9 to 12	20 ms	25 V
13 to 16	200 ms	25 V

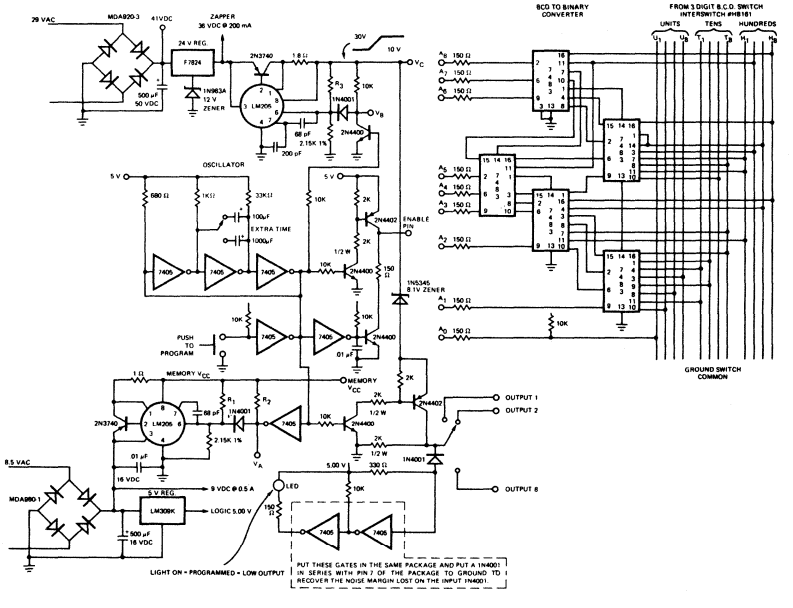
PROGRAMMER DESCRIPTION

Figure 5 below shows the curcuitry required to build a simple manual programmer. The operator with this programmer dials in the memory address to be programmed on a three digit thumbwheel switch and selects the output to be programmed or readout on an 8 position rotary switch. Pushing the program button will open the nichrome link at the selected address. When the program button is released the memory data is displayed on an LED.

OPERATION

Five 7483's are used to convert from BCD to binary addresses. An LM205 is used to control the device V_{CC} and vary it from 4.20 to 5.50 V depending upon whether V_A is high or low. V_A and V_B are controlled by the oscillator which is turned on when the program button is pushed. V_A and V_B vary the device V_{CC} and programming voltage by changing the resistor divider values on the LM205 which set the output voltage. Two oscillator speeds can be selected by a two position switch.

MANUAL PROGRAMMER



NOTES:

1. Adjust R_1 and R_2 so that the memory V_{CC} is 4.150 to 4.250 V quiescent and 5.450 to 5.550 V when the program button is pushed. $R_1 \approx 5K$, $R_2 \approx 15K$.
2. Adjust R_3 for 31 to 33 V on V_C when the program button is pushed. $V_C \approx \frac{R_3\ (k\Omega)}{2.15\ k}(1.7\ V)$ so $R_3 \approx 41K$.
3. Use Thermalloy heat sink #6166B on both 2N3740 transistors.

REQUIRED INFORMATION FOR MMI TO PROGRAM TO YOUR TRUTH TABLE

TRUTH TABLES

MMI can program devices at our facility from MMI truth table forms (available on request). For customers desiring to make their own forms, an example is shown below:

		OUTPUTS							
WORD	PIN →	17	16	15	14	13	11	10	9
NUMBER		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0		H	H	H	L	H	L	H	L
1		L	H	L	H	L	L	H	H
.		.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.
511 (255 ON THE 5335/6335)		L	H	H	H	H	L	H	L

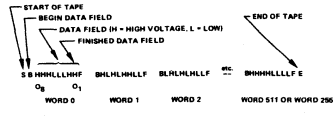
Note: A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pins, so for example, word 511 = HHHHHHHHH.

PAPER TAPE FORMAT

Truth tables can also be sent to MMI in. an ASCII tape format. Information can be sent to us by air mail or TWX 910-339-9224. The tape reading equipment at MMI only recognizes ASCII characters S, B, H, L, F and E and interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to the last word. Carriage returns should be included to permit listing on a printer.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or control characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is O_8 to O_1, not O_1 to O_8.

A typical list of characters and their machine interpretations are shown below:



The required heading information at the beginning of the tape is as follows:

CUSTOMERS NAME AND PHONE _____ TRUTH TABLE NUMBER _____

CUSTOMERS TWX NUMBER _____ NUMBER OF TRUTH TABLES _____

PURCHASE ORDER NUMBER _____ TOTAL NUMBER OF PARTS _____

MMI PART NUMBER _____ NUMBER OF PARTS OF EACH TRUTH TABLE _____

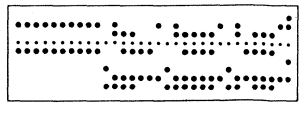
CUSTOMER SYMBOLIZED PART NUMBER _____ 25 BELL OR RUBOUT CHARACTERS _____

An example is shown below for a 256 x 4 Prom (6300)

BLARNEY ELECTRONICS 408-735-8104
TWX 911-338-9225
P0142
6300
0431
12
1
3
3

SBLLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF BLLLLF
BLLLLF BLHLHF BLLHHF BHHHLF BHHLLF BLLHHF BHHLLF BLLHHF BLHLHF

8 level
TWX



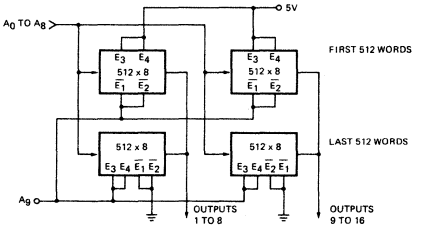
APPLICATION INFORMATION

MEMORY OPERATION

The memory is addressed with inputs A_0 through A_8 (A_0 to A_7 on the 5335/6335). An eight bit parallel readout is available for each word on outputs O_1 to O_8. To enable the outputs for a readout, enable $\overline{E_1}$ and $\overline{E_2}$ must be low and E_3 and E_4 must be high. If the chip is disabled, the outputs are held off permitting wire "OR"ing of the outputs of several packages. The use of the enable permits expansion to a greater number of words.

MEMORY EXPANSION 1024 X 16 SYSTEM

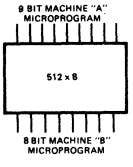
The highest order address (A_9) is used in conjunction with the chip enable to select either the first 512 words (when A_9 is low) or the last 512 words (when A_9 is high). The corresponding outputs of the packages in the same column are OR tied for the 16 bit readout required.



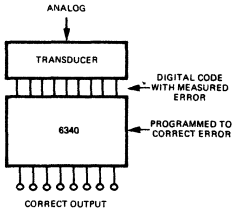
GENERAL

The P.ROM was designed for situations which require a fast turnaround on bit patterns. The device permits patterns to be changed in the field in minutes. The pin and performance compatibility with the mask programmable ROM permits fast prototyping and the economic advantages of mask made ROM. The interchangeability and side by side operation of the ROM and P.ROM offers an effective means of customizing a small portion of a machine, or permitting engineering changes, or eliminating field stocking of mask programmable ROMs.

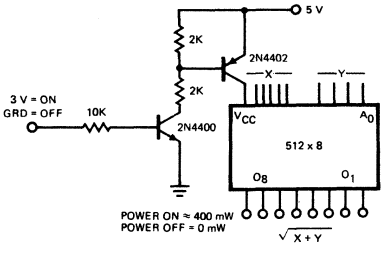
EMULATION

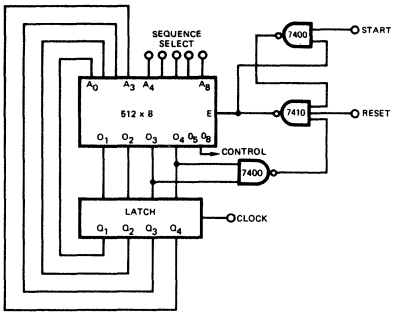


TRANSDUCER ERROR CORRECTION



LOW POWER FUNCTION GENERATION





ADDRESS	$A_8A_7A_6A_5A_4$	SEQUENCE NO.
0 TO 15	L L L L L	1) SERVICE TELETYPE
16 TO 31	L L L L L	2) SERVICE PRINTER
.	. . . . .	.
.	. . . . .	.
495 TO 511	H H H H H	31) SERVICE CASSETTE

The enable is used to define a known starting point since when it is high the memory outputs are high regardless of the programmed code.

F1 = $\overline{A}BCD + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$.

INTERPRETATION:

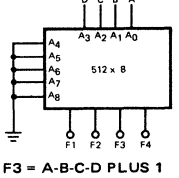
F1 is high if address 14, 13, 11 or 7 is selected

F2 = $\overline{A}\overline{B}CD + BC\overline{D}$

INTERPRETATION:

F2 is high if address 12, 7 or 6 is selected

NOTE: ONLY 16 WORDS AND 4 OUTPUTS OF THE 512 ARE USED. THE REST COULD BE USED FOR OTHER FUNCTIONS.



F3 = A-B-C-D PLUS 1

F4 = A-B-C-D MINUS 1

1024 BIT BIPOLAR (256 X 4) READ ONLY MEMORY

H5200/H6200 H5201/H6201

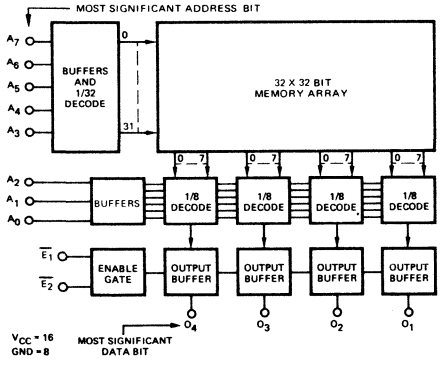
Monolithic Memories
INCORPORATED

PRODUCT FEATURES

- 45 ns Max. Access Time over 0°C to 75°C and ±5% Voltage Variation (H6200, H6201)
- 60 ns Max. Access Time over −55°C to 125°C and ±10% Voltage Variation (H5200, H5201)
- Advanced Schottky Processing
- Low Input Current (250 μA Max.)
- Single Layer Metal for Reliability
- Pin Compatible with 6200, 6300 ROM and PROM

	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
H6200		X		X
H6201		X	X	
H5200	X			X
H5201	X		X	

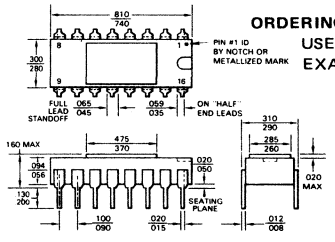
BLOCK DIAGRAM: 256 WORDS X 4 BITS MEMORY



PACKAGE OUTLINE

16 Pin Ceramic (Side Braze)

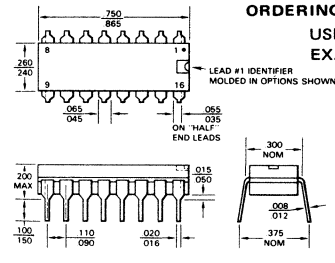
Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/ watt



ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE H6200D

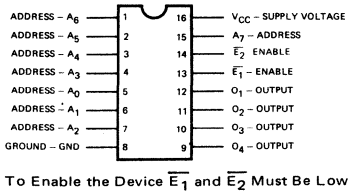
16 Pin Plastic

θ_{JA} ≈ 90° C/WATT
SOLDERED TO BOARD IN STILL AIR



ORDERING INFORMATION
USE THE SUFFIX N
EXAMPLE H6200 N

PIN CONFIGURATION



To Enable the Device $\overline{E_1}$ and $\overline{E_2}$ Must Be Low

APPLICATIONS MICROPROGRAMMING, CODE CONVERSION.

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

MARCH 1974

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V
Input Voltage	−1.2 to 7.0 V
Output Current	100 mA
Storage Temperature	−65 to 160°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability Functional operation at these limits is not guaranteed or implied

D.C. CHARACTERISTICS*

PARAMETER		CONDITIONS	H5200/H5201			H6200/H6201			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V			−250			−250	µA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			25			25	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 10 mA			0.50				V
		V_{CC} = Min, I_{OL} = 15 mA						0.50	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, Inputs GRD, Outputs Open		97	130		97	125	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current H5200/H6200 Only	V_{CC} = Max, V_{CEX} = 2.4 V			100			100	µA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA			−1.5			−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF
THREE STATE PARAMETERS H5201/H6201 ONLY									
I_{LZ}	Output Leakage High Impedance State	V_O = 0.50 V			−100			−100	µA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5 V	−20	−50	−85	−20	−50	−85	mA
I_{HZ}	Output Leakage High Impedance State	V_{CC} = Max, V_{CEX} = 2.40 V			100			100	µA
V_{OH}	Output Voltage "High"	I_O = −3.2 mA	2.4			2.4			V

* Unless otherwise indicated, all limits for the H6200/H6201 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the H5200/H5201 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C.

1. Typical values are measured at 5.0 V and 25°C.

A.C. CHARACTERISTICS WITH STANDARD LOAD (FIG. 1)

PARAMETER	SYMBOL	FIGURE	H5200/H5201 5 V ±10%, −55 to 125°C		H6200/H6201 5 V ±5%, 0 to 75°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	3	5	60	5	45
Enable Access Time	T_{EA}	2	5	35	5	35
Enable Recovery Time	T_{ER}	2	5	35	5	35
H5201/H6201 ONLY						
Chip Enable to Low Impedance Delay	T_{ON}		0		0	
Chip Enable to High Impedance Delay	T_{OFF}			30		35

FIGURE 1.
STANDARD LOAD

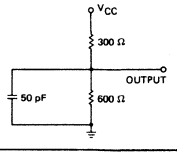


FIGURE 2.

Input Pulse Amplitude = 2.5 V
Input Rise and Fall Time
5 ns From 1 V to 2 V
Measurements Made at 1.50 V

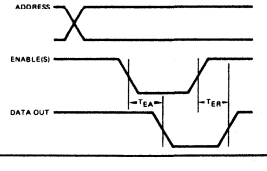
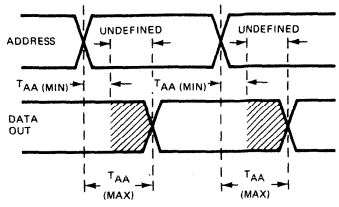


FIGURE 3.



PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 15 mA for the H6200
10 mA for the H5200
I_F = The maximum input load current of the TTL family at 0.50 V.
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four H6200 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 15 mA

$$R_L\ (max) = \frac{V_{CC}-2.40\ V}{M(100\ \mu A)+N(I_R)} \qquad R_L\ (max) = \frac{5.0-2.4\ V}{4\ (100\ \mu A) + 3\ (40\ \mu A)} = 5000\ ohms$$

$$R_L\ (min) = \frac{V_{CC}-0.50\ V}{I_{OL}-N(I_F)} \qquad R_L\ (min) = \frac{5.0-0.50\ V}{15\ mA-3(1.6\ mA)} = 441\ ohms$$

THREE-STATE OUTPUT – SEE FIGURES A AND B

FIGURE A
THREE-STATE OUTPUT

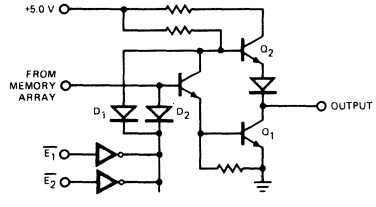
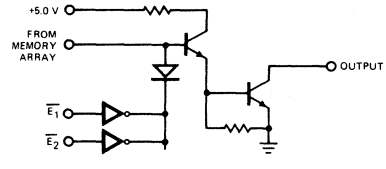


FIGURE B
OPEN COLLECTOR OUTPUT



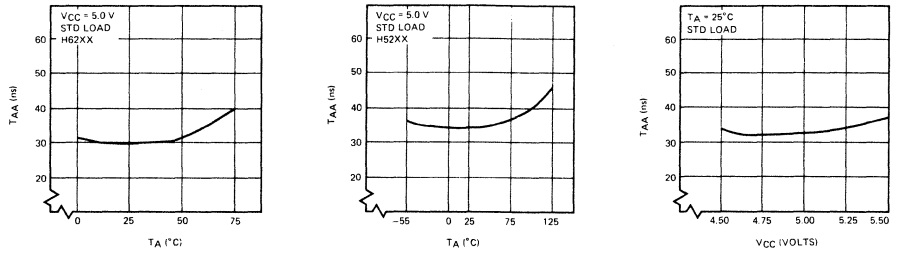
The three-state output of the H5201/H6201 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment, up to 33 memory outputs of the H5201/H6201 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

CHARACTERISTIC CURVES OF TYPICAL DEVICES

CURVES



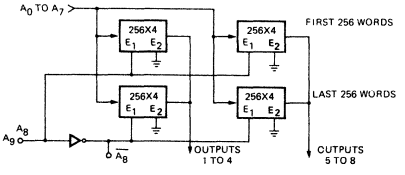
Note: The T_{EA} parameter typically varies from 15 to 25 ns for the H52XX/H62XX over voltage and temperature for 5.0 V ± 10%, −55 to 125° C.

MEMORY OPERATION

The memory is addressed with inputs A_0 through A_7 which select one of 256 words. A four bit parallel readout is available for each word on outputs O_1 to O_4. To enable the outputs for a readout, both enables $\overline{E_1}$ and $\overline{E_2}$ must be low. If either enable, or both, is high, the outputs are held off permitting wire "OR"ing of open collector of three state outputs of several packages. The use of the enables permits expansion to greater than 256 words.

MEMORY EXPANSION 512 X 8 SYSTEM

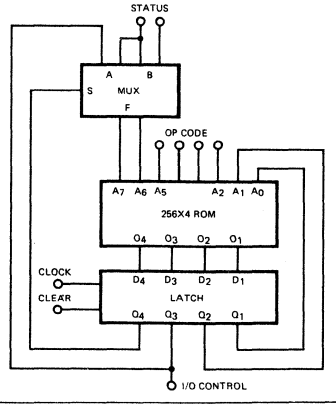
The highest order address (A_8) is used in conjunction with the chip enables to select either the first 256 words (when A_8 is low) or the last 256 words (when A_8 is high). The corresponding outputs of the packages in the same column are OR tied for the 8 bit readout required.



APPLICATIONS

The fast access time of the H52XX/H62XX makes it particularly suitable for microprogramming applications. The pin compatibility with the 6200 (256X4, 60 ns ROM) and 6300 (256X4 P.ROM) permit system upgrading to faster speeds plus easy prototyping.

MICROPROGRAMMING



BIPOLAR READ ONLY MEMORIES

5230/5231/6230/6231
5225/6225
5210/6210
5205/5206/6205/6206
5200/5201/6200/6201

Monolithic Memories
INCORPORATED

PRODUCT FEATURES

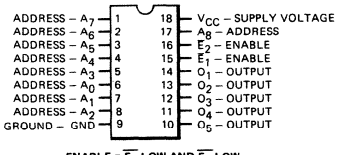
- Fully decoded — on chip address decoding
- DTL and TTL compatible
- The 2048 Bit, 1024 Bit, and 256 Bit ROMS are pin compatible with monolithic memories programmable ROMS

PART NUMBERS

SIZE	ORGANIZATION	OPEN COLLECTOR		THREE STATE	
		MILITARY	COMMERCIAL	MILITARY	COMMERCIAL
2560 BITS	512 X 5	5225	6225		
2048 BITS	512 X 4	5205	6205	5206	6206
1280 BITS	256 X 5	5210	6210		
1024 BITS	256 X 4	5200	6200	5201	6201
256 BITS	32 X 8	5230	6230	5231	6231

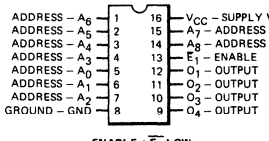
PIN CONFIGURATIONS

5225/6225



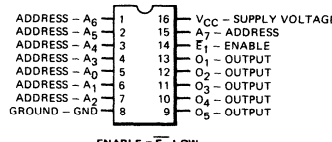
ENABLE = $\overline{E_1}$ LOW AND $\overline{E_2}$ LOW

5205/5206
6205/6206



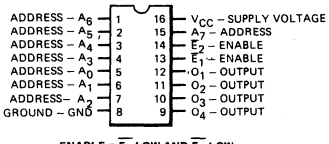
ENABLE = $\overline{E_1}$ LOW

5210/6210



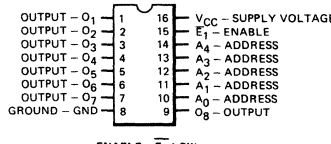
ENABLE = $\overline{E_1}$ LOW

5200/5201
6200/6201



ENABLE = $\overline{E_1}$ LOW AND $\overline{E_2}$ LOW

5230/5231
6230/6231



ENABLE = $\overline{E_1}$ LOW

APPLICATIONS Microprogramming, Code Conversion, Logic Replacement

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

MARCH 1974

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7.0 V
Input Voltage	−1.0 to 7.0 V
Output Current	100 mA
Storage Temperature	−65 to 160°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.
Functional operation at these limits is not guaranteed or implied.

D.C. CHARACTERISTICS:

Unless otherwise indicated, all limits for the 62XX are guaranteed for 5.0 V ±5% in a free air temperature of 0 to 75°C; all limits for the 52XX are guaranteed for 5.0 V ±10% in a free air temperature of −55 to 125°C.

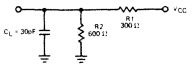
PARAMETER		CONDITIONS	52XX			62XX			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V			−1.6			−1.6	mA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			40			40	μA
		V_{CC} = Max, V_R = 4.50 V			1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 10 mA			0.45				V
		V_{CC} = Min, I_{OL} = 16 mA						0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V			125			125	mA
		5230/6230 Only		80	100		80	100	mA
V_{IL}	Low level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.40 V			100			100	μA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA			−1.5			−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1.0 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1.0 MHz Output in High State		8.0			8.0		pF
THREE STATE PARAMETERS — 5206/6206, 5201/6201, 5231/6231 ONLY									
I_{LZ}	Output Leakage High Impedance State	V_O = 0.50 V			−100			−100	μA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5.0 V	−20		−90	−20		−90	mA
I_{HZ}	Output Leakage High Impedance State	V_{CC} = Max, V_O = 2.40 V			100			100	μA
V_{OH}	Output Voltage HIGH	I_O = −3.2 mA for 62XX, I_o = −900 μA for 52XX	2.4			2.4			V

1. Typical values are measured at 5.0 V and 25°C.

A.C. CHARACTERISTICS — With Standard Load

PARAMETER		SYMBOL	FIGURE	52XX 5.0 V, 25°C		62XX 5.0 V, 25°C	
				MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time		T_{AA}	1				
	5225			20	100		
	6225					15	75
	5210			15	60		
	6210					15	75
	5205, 5206			15	90		
	6205, 6206					15	60
	5200, 5201			10	50		
	6200, 6201					10	50
	5230, 5231			10	50		
	6230, 6231					10	50
Enable Access Time and		T_{EA}	2				
Enable Recovery Time		T_{ER}	2				
	5225			5	50		
	6225					5	40
	5210			5	35		
	6210					5	30
	5205, 5206			5	50		
	6205, 6206					5	30
	5200, 5201			5	30		
	6200, 6201					5	30
	5230, 5231			5	30		
	6230, 6231					5	30

STANDARD TEST LOAD



Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 15 mA and 30 pF as given in std. load

Fig. 1
ADDRESS ACCESS TIME

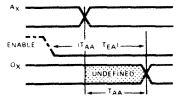
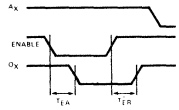


Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 16 mA for the 62XX
10 mA for the 52XX
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four 6230 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 16 mA

$$R_L(\text{max}) = \frac{V_{CC} - 2.4\text{ V}}{M(100\,\mu\text{A}) + N(I_R)} \qquad R_L(\text{max}) = \frac{5.0 - 2.4\text{ V}}{4(100\,\mu\text{A}) + 3(40\,\mu\text{A})} = 5000\text{ ohms}$$

$$R_L(\text{min}) = \frac{V_{CC} - 0.45\text{ V}}{I_{OL} - N(I_F)} \qquad R_L(\text{min}) = \frac{5.0 - 0.45\text{ V}}{16\text{ mA} - 3(1.6\text{ mA})} = 406\text{ ohms}$$

THREE-STATE OUTPUT — SEE FIGURES A AND B

FIGURE A
THREE STATE OUTPUT

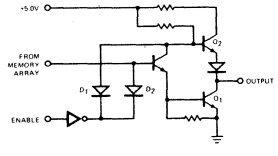
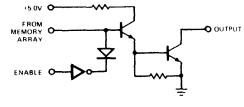


FIGURE B
OPEN-COLLECTOR OUTPUT



The three-state output offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip enable is low, D_{11} and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire O Ring of memory outputs. This condition is called the high impedance third state.

In a system environment, up to 33 memory outputs of the 6206, 6201, 6231 or 10 outputs of the 5206, 5201, 5231 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

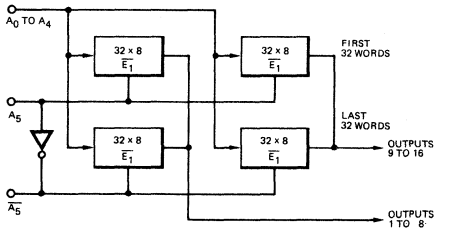
MEMORY INFORMATION AND PACKAGE OUTLINES

MEMORY OPERATION

The memory is addressed with inputs A_0 to A_N which selects one of the 2^n words. An "M" bit parallel readout is available for each output O_1 to O_M. To enable the outputs for a readout the enable(s) must be low. If one or more of the enable(s) is (are) high, the outputs are held off permitting wire "OR" ing of the outputs of several packages. The use of the enable(s) permit(s) expansion to more words than are available in a single package.

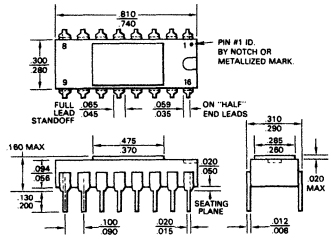
MEMORY EXPANSION EXAMPLE 64 X 16 SYSTEM

The highest order address (A_5) is used in conjunction with the chip enable to select either the first 32 words (when A_5 is low) or the last 32 words (when A_5 is high). The corresponding outputs of the packages in the same column are OR tied for the 16 bit readout required.



PACKAGE OUTLINES

16 PIN CERAMIC (SIDE BRAZE)

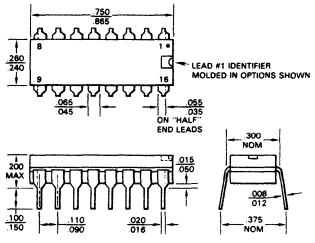


Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/watt

ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6230 D

16 PIN CERAMIC (CERDIP)

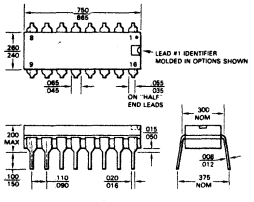


Θ_{JC} (thermal resistance from junction to junction to case with freon as a heat sink) ≈ 24°C/watt

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 75°C/watt

ORDERING INFORMATION
USE THE SUFFIX J
EXAMPLE 6230J

16 PIN PLASTIC

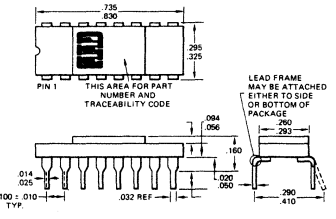


Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 90°C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 36°C/watt

ORDERING INFORMATION
USE THE SUFFIX N
EXAMPLE 6230N

18 PIN CERAMIC 5225/6225 ONLY



Θ_{JC} (thermal resistance from junction to junction to case with freon as a heat sink) ≈ 20°C/watt

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 67°C/watt

ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6225 D

8192 BIT (1024×8) AND 4096 BIT (512×8) BIPOLAR READ ONLY MEMORIES

A5280/A6280
A5281/A6281
A5240/A6240
A5241/A6241

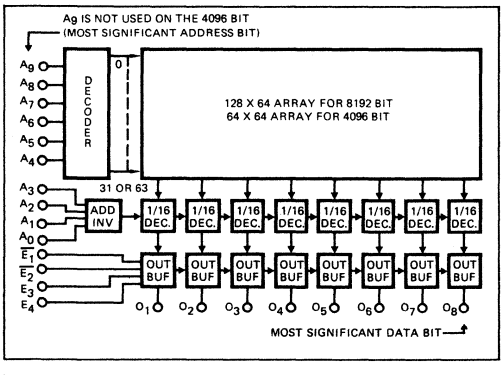
Monolithic Memories
INCORPORATED

PRODUCT FEATURES

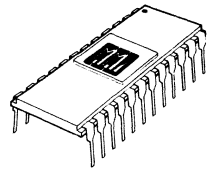
- Advanced Schottky Processing
- Low Power Dissipation
- Fast Access Time: 150 ns Max.
- Totally TTL Compatible
- Fully Decoded On Chip Address Decoding
- Low Input Current (250 μA Max)
- Four Enable Inputs Allow Memory Expansion
- Open Collector or Three State Outputs

	MILITARY	COMMERCIAL	OPEN COLLECTOR	THREE STATE	8192 BIT (1024x8)	4096 BIT (512x8)
A5280	X		X		X	
A5281	X			X	X	
A6280		X	X		X	
A6281		X		X	X	
A5240	X		X			X
A5241	X			X		X
A6240		X	X			X
A6241		X		X		X

BLOCK DIAGRAM

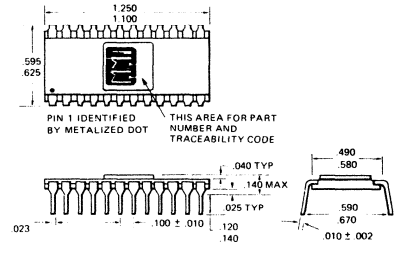


PACKAGE CONFIGURATION



PACKAGE OUTLINE

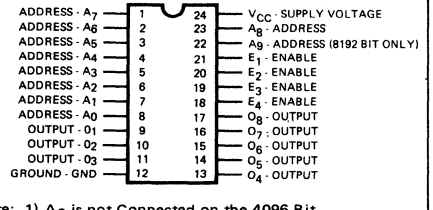
Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 48°C/watt



ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE A6281D

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt.

PIN CONFIGURATION



Note: 1) A_9 is not Connected on the 4096 Bit
2) The Chip is Enabled when $\overline{E_1}$ and $\overline{E_2}$ are Low and E_3 and E_4 are High.

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

MARCH 1974

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V
Input Voltage	−1.0 to 5.5 V
Output Current	100 mA
Ambient Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.

D.C. CHARACTERISTICS

Unless otherwise indicated, all limits for the A62XX are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the A52XX are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C

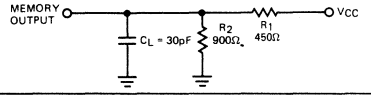
PARAMETER		CONDITIONS	A52XX			A62XX			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V			−250			−250	µA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			25			25	µA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 8 mA			0.50				V
		V_{CC} = Min, I_{OL} = 10 mA						0.50	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, Chip Disabled All Outputs Open		110	140		110	140	mA
		V_{CC} = 5.0 V, Chip Enabled All Outputs Open		130	170		130	170	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current (Open Collector Only)	V_{CC} = Max, V_{CEX} = 2.40 V High Stored or Disabled			100			100	µA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA		−1.0	−1.5		−1.0	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF
THREE STATE PARAMETERS — A5241, A6241, A5281, A6281 ONLY									
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5 V	−20	−50	−90	−20	−50	−90	mA
I_{HZ}	Output Leakage High Impedance State	V_{CC} = Max, V_O = 0.45 V to 2.40 V Chip Disabled			±50			±50	µA
V_{OH}	Output Voltage "High"	I_O = −700 µA for the A6281, A6241 I_O = −500 µA for the A5281, A5241	2.4	3.2		2.4	3.2		V

1. Typical values are measured at 5.0 V and 25°C

A.C. CHARACTERISTICS With Standard Load

PARAMETER	SYMBOL	FIGURE	A52XX 5.00 V, 25°C		A62XX 5.00 V, 25°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	1	20	175	20	175
Enable Access Time	T_{EA}	2	10	70	10	70
Enable Recovery Time	T_{ER}	2	10	70	10	70
Chip Enable to Low Impedance Delay	T_{ON}		10		10	
Chip Enable to High Impedance Delay	T_{OFF}			70		70

STANDARD TEST LOAD



Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V

TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

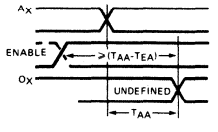
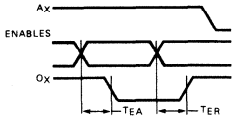


Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME

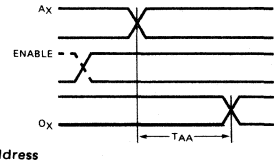


Ax = Any Address
Ox = Any Output

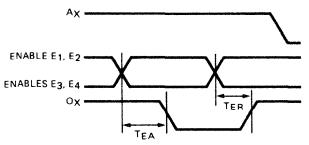
APPLICATION INFORMATION

TEST WAVEFORMS

ADDRESS ACCESS TIME



ENABLE ACCESS TIME AND RECOVERY TIME



A_X = Any Address
O_X = Any Output

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR DEVICES

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 10 mA for the A6280, A6240
8 mA for the A5280, A5240
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example: Four A6280 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V.

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 10 mA

$$R_L(\text{max}) = \frac{V_{CC} - 2.40\ V}{M(100\ \mu A) + N(I_R)} \qquad R_L(\text{max}) = \frac{5.0 - 2.4\ V}{4\ (100\ \mu A) + 3\ (40\ \mu A)} = 5000 \text{ ohms}$$

$$R_L(\text{min}) = \frac{V_{CC} - 0.45\ V}{I_{OL} - N(I_F)} \qquad R_L(\text{min}) = \frac{5.0 - 0.45\ V}{10\ mA - 3(1.6\ mA)} = 875 \text{ ohms}$$

USE OF CUSTOM ROM TRUTH TABLE FORM

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below:

WORD NUMBER	PIN	17 O_8	16 O_7	15 O_6	14 O_5	13 O_4	11 O_3	10 O_2	9 O_1
0		L	H	L	H	H	L	L	L
1		H	H	L	L	H	L	H	L
•		•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•
1023		L	L	H	H	H	L	L	L

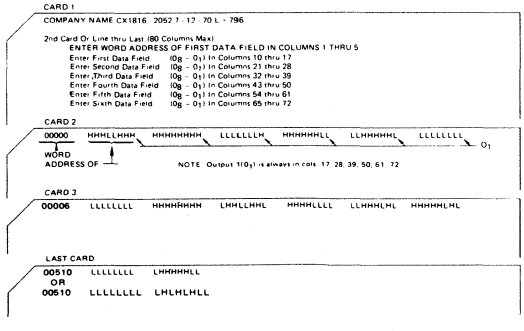
511 for 4096 Bit

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 1023 = HHHHHHHHHH.

PUNCHED CARD OR TAPE FORMAT

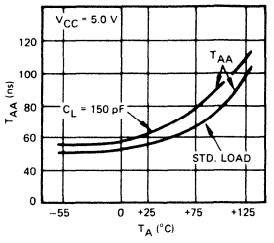
PUNCHED CARD OR TAPE FORMAT

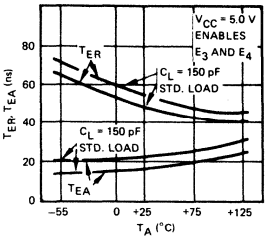
1st Card or Line (80 Columns Max): Enter Company Name – Part Number – Date – Number of "L's" In Pattern
(Free Form Entry No Commas) [Paper Tape Format, Terminate each Line with Carriage Return and Linefeed]

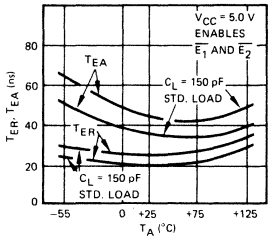


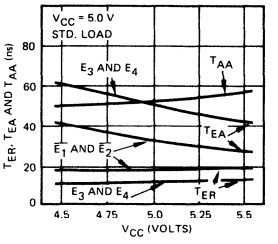
NOTE:
Leading edge zeros in the word number may be eliminated. Columns 73 thru 80 are for comments.

APPLICATION INFORMATION









MEMORY OPERATION

The memory addressing uses inputs A_0 through A_N which select 1 of 2^{n+1} words for read out of eight bits on the outputs (O_1 –O_8). Larger memory sizes can be built by driving the additional package with the address lines and using the enables to selectively activate a particular package. The memory is enabled when E_1 and E_2 are logic "0" (low) and E_3 and E_4 are logic "1" (high). Logic equation enable = $E_1 \cdot E_2 \cdot E_3 \cdot E_4$.

THREE-STATE OUTPUT – SEE FIGURES A AND B

FIGURE A
THREE-STATE OUTPUT

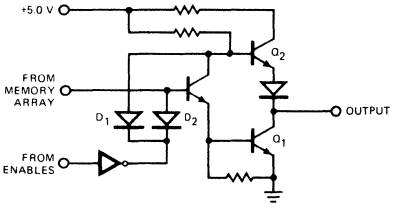
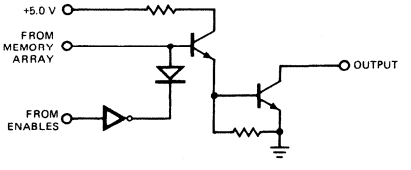


FIGURE B
OPEN COLLECTOR OUTPUT



The three-state output offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip is activated, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip is deactivated, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment,11 memory outputs of the A5281, A5241 or 15 memory outputs of the A6281, A6241 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

APPLICATIONS

The high bit density and the high speed make the ROMs especially suited for microprogramming, arithmetic functions, logic functions and character generators. For your custom bit pattern requirements use MMI standard tape, punch cards or custom bit pattern format.

2-4/10M/N

Monolithic Memories
INCORPORATED

HIGH SPEED 4096 BIT BIPOLAR (512 X 8) READ ONLY MEMORY

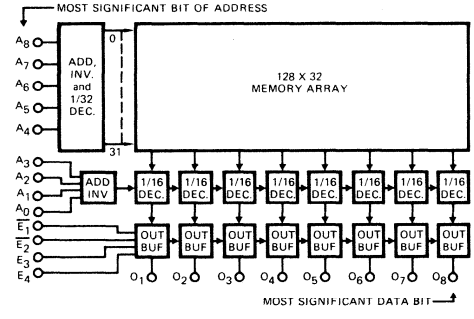
H5240/H5241
H6240/H6241

PRODUCT FEATURES

- Advanced Schottky Processing
- Low Power Dissipation 140 μW/bit
- Fast Access Time
- Totally TTL Compatible
- Fully Decoded On Chip Address Decoding
- Low Input Current (250 μA Max)
- Four Enable Inputs Allow Memory Expansion
- Open Collector/Three State Outputs
- Specified Over A Full –55° to +125°C Temp. Range

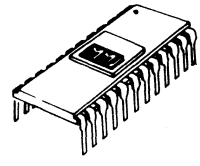
	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
H6240		X		X
H6241		X	X	
H5240	X			X
H5241	X		X	

BLOCK DIAGRAM: 512 WORDS X 8 BITS MEMORY



V_{CC} = 24
GND = 12

PACKAGE CONFIGURATION

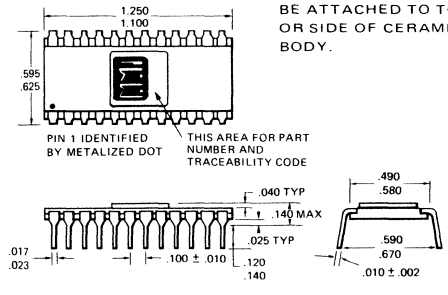


PACKAGE OUTLINE

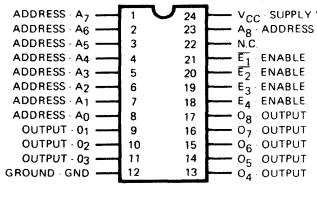
16 Pin Ceramic (Side Braze)

$\theta_{JA} \approx 60°C/WATT$ SOLDERED TO BOARD IN STILL AIR

NOTE: LEAD FRAME MAY BE ATTACHED TO TOP OR SIDE OF CERAMIC BODY.



PIN CONFIGURATION



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TWX 910–339-9229

SEPTEMBER 1974

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V
Input Voltage	−1.5 to 5.5 V
Output Current	100 mA
Ambient Temperature	−55 to +125°C
Storage Temperature	−65 to +150°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.

D.C. CHARACTERISTICS* Memory outputs are open collector and three-state

* Unless otherwise indicated all limits apply for V_{CC} = 5.0 V ±5%, T_A = 0°C to 75°C for the H624X and V_{CC} = 5 V ±10%, T_A −55°C to 125°C for the H524X.

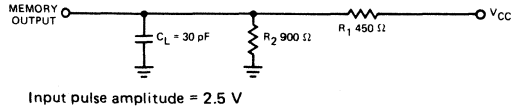
PARAMETER		CONDITIONS	H5240/41 MIN.	H5240/41 TYP.[1]	H5240/41 MAX.	H6240/41 MIN.	H6240/41 TYP.[1]	H6240/41 MAX.	UNITS
I_F	Input Load Current All Inputs	V_{CC} = Max, V_I = 0.45 V			−250			−250	µA
I_R	Input Leakage Current	V_{CC} = Max, V_I = 2.4 V			10			10	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 8.0 mA			0.50				V
		V_{CC} = Min, I_{OL} = 10 mA						0.50	V
I_{CC}	Power Supply Current (2)	Chip Disabled (3)		110	140		110	140	mA
		Chip Enabled		130	170		130	170	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.8			0.8	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA			−1.5			−1.5	V
BV_I	Breakdown Voltage All Inputs	V_{CC} = Max, I_I = 1.0 mA	5.0			5.0			V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V		5.0			5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V		7.0			7.0		pF
THREE STATE OUTPUT ONLY									
I_{LZ}	Output Leakage High Impedance State	V_O = 0.45 V			−100			−100	µA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5.0 V	−20		−85	−20		−85	mA
I_{HZ}	Output Leakage High Impedance State	V_O = 2.40 V			100			100	µA
V_{OH}	Output Voltage "High"	I_O = −900 µA	2.4			2.4			V
OPEN COLLECTOR OUTPUT ONLY									
I_{CEX}	Output Leakage Current	V_{CC} = 5.0 V = V_{CEX}			100			100	µA

NOTE: (1) Typical values are measured at 5.0 V and 25°C. (2) I_{CC} typically increases 5 mA at 5.25 V and 10 mA at 5.5 V over the 5.0 V value. (3) I_{CC} max H5241/H6241=170 mA disabled.

GUARANTEED LIMITS @ T_A = 25°C, V_{CC} = 5.00 V, STANDARD LOAD

PARAMETER	SYMBOL	FIGURE	H5240/41 MIN.	H5240/41 TYP.	H5240/41 MAX.	H6240/41 MIN.	H6240/41 TYP.	H6240/41 MAX.
Address Access Time (ns)	T_{AA}	1			90			75
Enable Access Time (ns)	T_{EA}	2			65			50
Enable Recovery Time (ns)	T_{ER}	2			30			30
Chip Enable to Low Impedance Delay (ns)				5			5	
Chip Enable to High Impedance Delay (ns)					70			60

STANDARD TEST LOAD

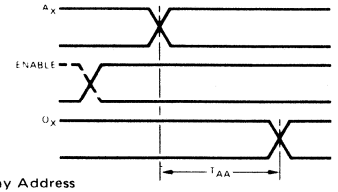


Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5 ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 10 mA and 30 pF as given in std. load

APPLICATION

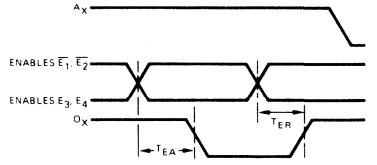
TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME



A_X = Any Address
O_X = Any Output

Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



USE OF CUSTOM ROM TRUTH TABLE FORM

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below:

WORD NUMBER	PIN	17 O_8	16 O_7	15 O_6	14 O_5	13 O_4	11 O_3	10 O_2	9 O_1
0		L	H	L	H	H	L	L	L
1		H	H	L	L	H	L	H	L
•		•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•
511		L	L	H	H	H	L	L	L

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.

PUNCHED CARD OR TAPE FORMAT

PUNCHED CARD OR TAPE FORMAT

1st Card or Line (80 Columns Max): Enter Company Name – Part Number – Date – Number of "L's" In Pattern
(Free Form Entry No Commas) [Paper Tape Format, Terminate each Line with Carriage Return and Linefeed]

CARD 1

COMPANY NAME CX1816 - 2052 7 - 12 - 70 L = 796

2nd Card Or Line thru Last (80 Columns Max)
ENTER WORD ADDRESS OF FIRST DATA FIELD IN COLUMNS 1 THRU 5
Enter First Data Field ($O_8 - O_1$) In Columns 10 thru 17
Enter Second Data Field ($O_8 - O_1$) In Columns 21 thru 28
Enter Third Data Field ($O_8 - O_1$) In Columns 32 thru 39
Enter Fourth Data Field ($O_8 - O_1$) In Columns 43 thru 50
Enter Fifth Data Field ($O_8 - O_1$) In Columns 54 thru 61
Enter Sixth Data Field ($O_8 - O_1$) In Columns 65 thru 72

CARD 2

00000 HHHLLHHH HHHHHHHH LLLLLLLH HHHHHHLL LLHHHHHL LLLLLLLL O_1

WORD ADDRESS OF

NOTE: Output 1(O_1) is always in cols. 17, 28, 39, 50, 61, 72

CARD 3

00006 LLLLLLLL HHHHHHHH LHHLLHHL HHHHLLLL LLHHHLHL HHHHHLHL

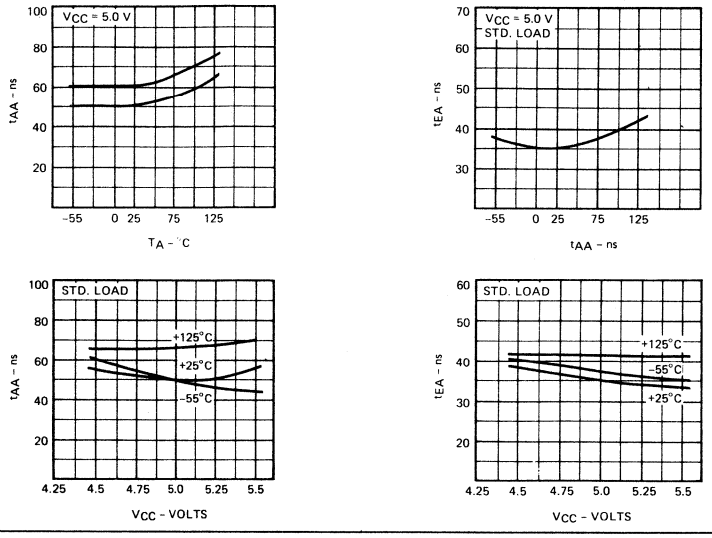
LAST CARD

00510 LLLLLLLL LHHHHHLL

NOTE:
Leading edge zeros in the word number may be eliminated. Columns 73 thru 80 are for comments.

CHARACTERISTIC CURVES

H5241 - TYPICAL AC CHARACTERISTICS



MEMORY OPERATION

The memory addressing uses inputs A_0 through A_8 which select 1 of 512 words for read out of eight bits on the outputs (O_1–O_8). Additional blocks of eight bits by 512 words may be added by driving additional packages with the respective address and enable lines. The memory is enabled when $\overline{E_1}$ and $\overline{E_2}$ are logic "0" (low) and E_3 and E_4 are logic "1" (high). Logic equation enable = $\overline{E_1} \cdot \overline{E_2} \cdot E_3 \cdot E_4$.

THREE-STATE OUTPUT — SEE FIGURES A AND B

FIGURE A
THREE STATE OUTPUT

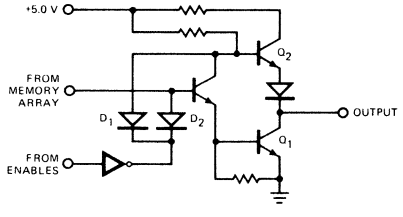
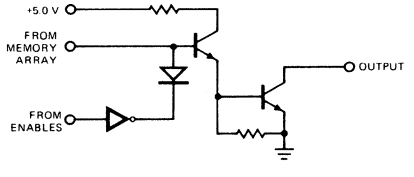


FIGURE B
OPEN COLLECTOR OUTPUT



The three-state output of the H5241/H6241 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip is activated, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip is deactivated, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment, ten memory outputs of the H5241/H6241 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

APPLICATIONS

The high bit density and the high speed make the H5241/H6241 especially suited for microprogramming, arithmetic functions, logic functions and character generators. For your custom bit pattern requirements use MMI standard tape, punch cards or custom bit pattern format.

9216 BIT BIPOLAR (1024 X 9) READ ONLY MEMORY

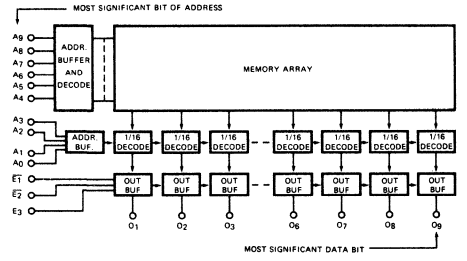
5260/6260

Monolithic Memories
INCORPORATED

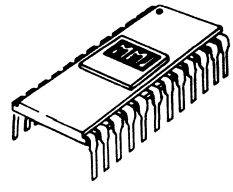
PRODUCT FEATURES

- **High bit density in a single package**
- **Low power dissipation. Typically 50 μw/bit**
- **Fast access time. 150 ns max.**
- **Low input current (250 μA max.)**
- **DTL and TTL compatible**
- **Three enable inputs allow memory expansion**
- **Advanced schottky processing**
- **Open collector outputs**

BLOCK DIAGRAM: 1024 WORDS X 9 BITS MEMORY



PACKAGE CONFIGURATION

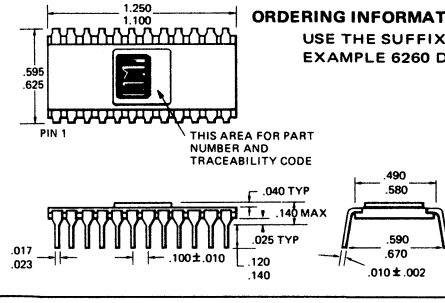


PACKAGE OUTLINE

24 Pin Ceramic

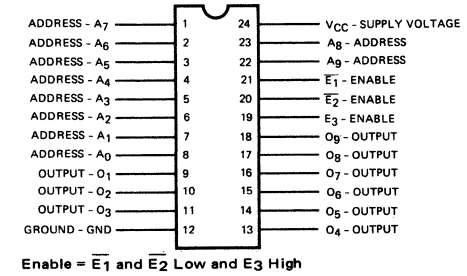
Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/watt

Θ_{JA} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt



ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6260 D

PIN CONFIGURATION



Enable = $\overline{E1}$ and $\overline{E2}$ Low and E3 High

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

NOVEMBER 1973

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V
Input Voltage	−1.0 to 5.5 V
Output Current	100 mA
Input Current	−20 to 5 mA
Storage Temperature	−65 to +150°C

Stresses above or extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.

D.C. CHARACTERISTICS:

Unless otherwise indicated, all limits for the 6260 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5260 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C

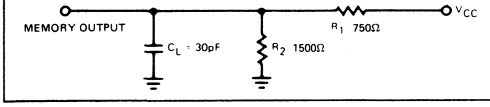
PARAMETER		CONDITIONS	5260			6260			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All inputs	V_{CC} = Max, V_F = 0.45 V			−250			−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 6 mA		0.35	0.50				V
		V_{CC} = Min, I_{OL} = 6 mA					0.35	0.50	V
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs at 2.4 V All Outputs Open		90	150		90	150	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.40 V			100			100	μA
	High Stored or Disabled	V_{CC} = Max = V_{CEX}			1			1	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5 mA		1.0	−1.5		−1.0	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF

1. Typical values are measured at 5.0 V and 25°C.

A.C. CHARACTERISTICS — With Standard Load

PARAMETER	SYMBOL	FIGURE	5260 5.00 V, 25°C		6260 5.00 V, 25°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	1	20	150	20	150
Enable Access Time	T_{EA}	2	10	60	10	60
Enable Recovery Time	T_{ER}	2	10	60	10	60

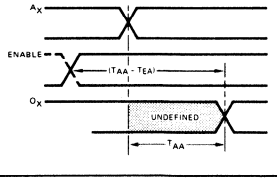
STANDARD TEST LOAD



Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 6 mA and 30 pF as given in std. load

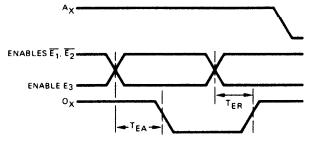
TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME



A_X = Any Address
O_X = Any Output

Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



APPLICATION

USE OF CUSTOM ROM TRUTH TABLE FORM

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below:

WORD NUMBER	PIN	OUTPUTS 18 O_9	17 O_8	16 O_7	15 O_6	14 O_5	13 O_4	11 O_3	10 O_2	9 O_1
0		L	L	H	L	H	H	L	L	L
1		H	H	H	L	L	H	L	H	L
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
1023		H	L	L	H	H	H	L	L	L

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 1023 = HHHHHHHHHH.

PUNCHED CARD OR TAPE FORMAT

Punched Card Or Tape Format

1st Card or Line (80 Columns Max): Enter Company Name – Part Number – Date - Number of "L's" In Pattern
(Free Form Entry No Commas) (Paper Tape Format, Terminate each Line with Carriage Return and Linefeed)

CARD 1

COMPANY NAME CX1816 - 2052 7 - 12 - 70 L = 796

2nd Card Or Line thru Last (80 Columns Max)
ENTER WORD ADDRESS OF FIRST DATA FIELD IN COLUMNS 1 THRU 5
Enter First Data Field ($O_9 - O_1$) In Columns 9 thru 17
Enter Second Data Field ($O_9 - O_1$) In Columns 20 thru 28
Enter Third Data Field ($O_9 - O_1$) In Columns 31 thru 39
Enter Fourth Data Field ($O_9 - O_1$) In Columns 42 thru 50
Enter Fifth Data Field ($O_9 - O_1$) In Columns 53 thru 61
Enter Sixth Data Field ($O_9 - O_1$) In Columns 64 thru 72

CARD 2

00000 HHHHLLHHH HHHHHHHHH LLLLLLLLH LHHHHHHLL LLLHHHHHL HLLLLLLLL O_1

WORD ADDRESS OF

Note: Output 1 (O_1) is always in cols. 17,28,39,50,61,72

CARD 3

00006 HLLLLLLLL LHHHHHHHH HLHHLLHHL LHHHHLLLL LLLHHHLHL LHHHHHLH

LAST CARD

01020 HLLLLLLLL HLHHHHHLL HLHLHLHLH LHLHLLHHH

NOTE:
Leading edge zeroes in the word number may be eliminated. Columns 73 thru 80 are for comments.

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 6 mA for the 5260/620
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:

Four 6260 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 6 mA

$$R_L(\text{max}) = \frac{V_{CC} - 2.40\ V}{M(100\ \mu A) + N(I_R)} \qquad R_L(\text{max}) = \frac{5.0 - 2.4\ V}{4(100\ \mu A) + 3(40\ \mu A)} = 5000 \text{ ohms}$$

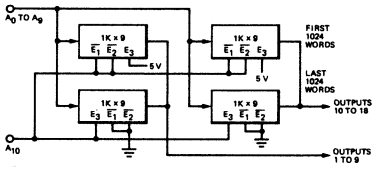
$$R_L(\text{min}) = \frac{V_{CC} - 0.50\ V}{I_{OL} - N(I_F)} \qquad R_L(\text{min}) = \frac{5.0 - 0.50\ V}{6\ mA - 3(1.6\ mA)} = 3750 \text{ ohms}$$

MEMORY OPERATION

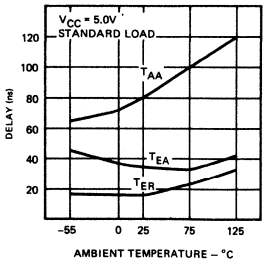
The memory is addressed with inputs A_0 through A_9. A nine bit parallel readout is available for each word on outputs O_1 to O_9. To enable the outputs for a readout, enable $\overline{E_1}$ and $\overline{E_2}$ must be low and E_3 must be high. If the chip is disabled, the outputs are held off permitting wire "OR"ing of the outputs of several packages. The use of the enable permits expansion to a greater number of words.

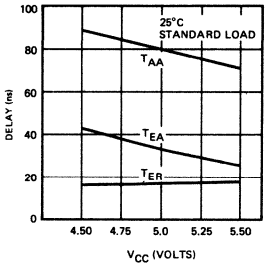
MEMORY EXPANSION – 2048 X 18 SYSTEM

The highest order address (A_{10}) is used in conjunction with the chip enable to select either the first 1024 words (when A_{10} is high). The corresponding outputs of the packages in the same column are OR tied for the 18 bit readout required.



CHARACTERISTIC CURVES





10240 BIT BIPOLAR (1024 x 10) READ ONLY MEMORY

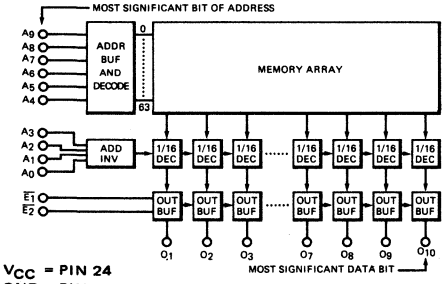
5255/6255

Monolithic Memories
INCORPORATED

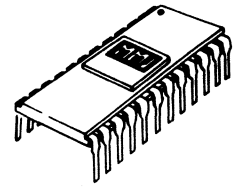
PRODUCT FEATURES

- High Bit Density in a Single Package
- Low Power Dissipation. Typically 50 μw/bit
- Fast Access Time. 150 ns max.
- Low Input Current (250 μA max.)
- DTL and TTL Compatible
- Two Enable Inputs Allow Memory Expansion
- Advanced Schottky Processing
- Open Collector Outputs

BLOCK DIAGRAM: 1024 WORDS X 10 BITS MEMORY



PACKAGE CONFIGURATION

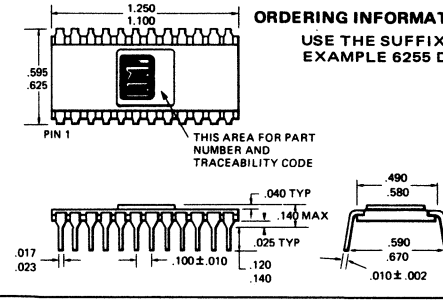


PACKAGE OUTLINE

24 Pin Ceramic

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/watt

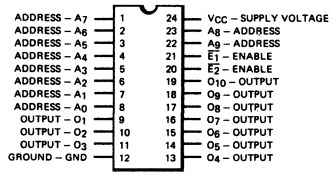
Θ_{JA} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt



ORDERING INFORMATION

USE THE SUFFIX D
EXAMPLE 6255 D

PIN CONFIGURATION



Enable = $\overline{E_1}$ and $\overline{E_2}$ Low

Monolithic Memories
INCORPORATED

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TWX 910–339-9229

NOVEMBER 1973

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V
Input Voltage	−1.0 to 5.5 V
Output Current	100 mA
Input Current	−20 to 5 mA
Storage Temperature	−65 to +150°C

Stresses above or extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.

D.C. CHARACTERISTICS:

Unless otherwise indicated, all limits for the 6255 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5255 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C

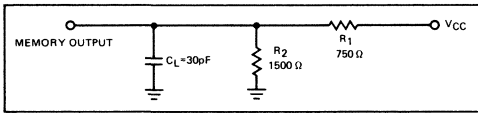
PARAMETER		CONDITIONS	5255			6255			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All inputs	V_{CC} = Max, V_F = 0.45 V			−250			−250	µA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			25			25	µA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 6 mA		0.35	0.50				V
		V_{CC} = Min, I_{OL} = 6 mA					0.35	0.50	V
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs at 2.4 V All Outputs Open		90	150		90	150	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.40 V			100			100	µA
	High Stored or Disabled	V_{CC} = Max = V_{CEX}			1			1	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5 mA		1.0	−1.5		−1.0	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF

1. Typical values are measured at 5.0 V and 25°C.

A.C. CHARACTERISTICS — With Standard Load

PARAMETER	SYMBOL	FIGURE	5255 5.00 V, 25°C		6255 5.00 V, 25°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	1	20	150	20	150
Enable Access Time	T_{EA}	2	10	60	10	60
Enable Recovery Time	T_{ER}	2	10	60	10	60

STANDARD TEST LOAD



Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5 ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 6 mA and 30 pF as given in std. load

TEST WAVEFORMS

FIGURE 1

ADDRESS ACCESS TIME

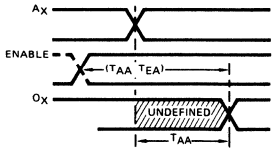
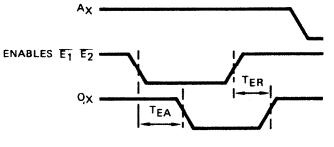


FIGURE 2

ENABLE ACCESS TIME AND RECOVERY TIME



AX = Any Address
OX = Any Output

USE OF CUSTOM ROM TRUTH TABLE FORM

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below:

WORD NUMBER	PIN	OUTPUTS 19 O_{10}	18 O_9	17 O_8	16 O_7	15 O_6	14 O_5	13 O_4	11 O_3	10 O_2	9 O_1
0		H	L	L	H	L	H	H	L	L	L
1		L	H	H	H	L	L	H	L	H	L
•		•	•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•	•
1023		H	H	L	L	H	H	H	L	L	L

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 1023 = HHHHHHHHHH.

PUNCHED CARD OR TAPE FORMAT

Punched Card Or Tape Format

1st Card or Line (80 Columns Max.): Enter Company Name – Part Number – Date – Number of "L's" In Pattern
(Free Form Entry No Commas) (Paper Tape Format, Terminate each Line with Carriage Return and Linefeed)

CARD 1

COMPANY NAME CX1816–2052 7–12–70 L=796

2nd Card Or Line thru Last (80 Columns Max.)
ENTER WORD ADDRESS OF FIRST DATA FIELD IN COLUMNS 1 THRU 5
Enter First Data Field (O_{10}–O_1) In Columns 8 thru 17
Enter Second Data Field (O_{10}–O_1) In Columns 19 thru 28
Enter Third Data Field (O_{10}–O_1) In Columns 30 thru 39
Enter Forth Data Field (O_{10}–O_1) In Columns 41 thru 50
Enter Fifth Data Field (O_{10}–O_1) In Columns 52 thru 61
Enter Sixth Data Field (O_{10}–O_1) In Columns 63 thru 72

CARD 2

00000 LHHHHLLHHH LHHHHHHHHH LLLLLLLLLH LLHHHHHHLL HLLLHHHHHL LHLLLLLLLL

WORD ADDRESS OF

O_1

NOTE: Output 1 (O_1) is always in cols. 17,28,39,50,61,72

CARD 3

00006 LHLLLLLLLL HLHHHHHHHH LHLHHLLHHL HLHHHHLLLL LLLLHHHLHL HLHHHHHLH

LAST CARD

01020 HLLLLLLLL HHLHHHHHLL LHLHLHLHLH LLHLHLLHHH

NOTE: Leading edge zeroes in the word number may be eliminated. Columns 73 thru 80 are for comments.

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 6 mA for the 5255/6255
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

EXAMPLE:
Four 6255 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistor at V_{CC} = 5.0 V.

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 6 mA

$$R_L(\max) = \frac{V_{CC} - 2.40\ V}{M(100\ \mu A) + N(I_R)} \qquad R_L(\max) = \frac{5.0 - 2.4\ V}{4(100\ \mu A) + 3(40\ \mu A)} = 5000 \text{ ohms}$$

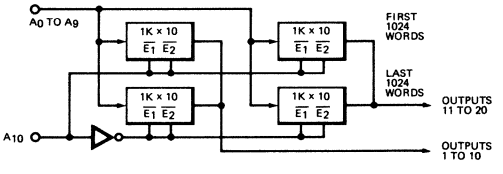
$$R_L(\min) = \frac{V_{CC} - 0.50\ V}{I_{OL} - N(I_F)} \qquad R_L(\min) = \frac{5.0 - 0.50\ V}{6\ mA - 3(1.6\ mA)} = 3750 \text{ ohms}$$

MEMORY OPERATION

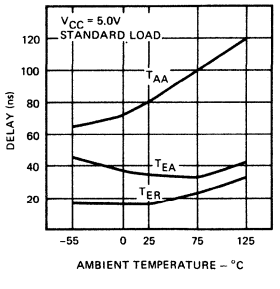
The memory is addressed with inputs A_0 through A_9. A ten bit parallel readout is available for each word on outputs O_1 to O_{10}. To enable the outputs for a readout, enable $\overline{E_1}$ and $\overline{E_2}$ must be low. If the chip is disabled, the outputs are held off permitting wire "OR"ing of the outputs of several packages. The use of the enable permits expansion to a greater number of words.

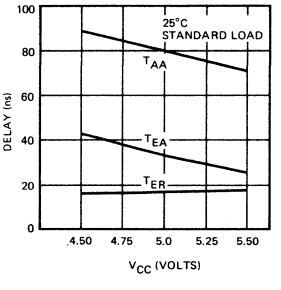
MEMORY EXPANSION (2048 X 20 SYSTEM)

The highest order address (A_{10}) is used in conjunction with the chip enable to select either the first 1024 words (when A_{10} is high). The corresponding outputs of the packages in the same column are OR tied for the 20 bit readout required.



CHARACTERISTIC CURVES





READ ONLY MEMORY

Monolithic Memories
INCORPORATED

SPECIAL NOTICE (effective 8/1/72)

1. Identify all pin positions.

Example Only:	Outputs =	O_8	O_7	O_6	O_5 or O_5	O_6	O_7	O_8
	Pins =	12	11	10	9 or 9	10	11	12

2. Define output logic in terms of H (high) or L (low) voltage levels.
3. List all addresses in decimal form.
4. Define address (input) logic in terms of H (high) or L (low) voltage levels.

Example:	0 = low	1 = high	Positive Logic
	0 = high	1 = low	Negative Logic

5. State total number of lows.

CUSTOM BIT PATTERN

Customer Name _____

Location _____

Customer Part No. _____ Rev. No. _____

Total Number of Output Lows ("L"or "1") Per Pattern = _____

Monolithic Memories Part Number _____

Customer Marking _____

Approved By _____ Date _____

Order Information

NOTE:
Words are numbered 0 through N and are addressed using sequential addressing of Address Leads A_0 through A_M with A_0 as as the least significant digit.

EXAMPLE:

WORD	A_M		A_6	A_5	A_4	A_3	A_2	A_1	A_0
WORD 0	0	— — —	0	0	0	0	0	0	0
WORD 1	0	— — —	0	0	0	0	0	0	1
WORD 2	0	— — —	0	0	0	0	0	1	0
WORD 3	0	— — —	0	0	0	0	0	1	1
| |	|	|	|	|	|	|	|	|	|
| |	|	|	|	|	|	|	|	|	|
| |	|	|	|	|	|	|	|	|	|
WORD N	1	— — —	1	1	1	1	1	1	1

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1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

ROM FORMAT

USE OF CUSTOM ROM TRUTH TABLE FORMS

All MMI products having 4 or 5 outputs should utilize the truth table listed on the 5 column (O_5 to O_1) form. The four output devices should use columns O_4 to O_1 leaving O_5 blank. Each truth table page accommodates up to 128 words.

All MMI products having 8 to 10 outputs should utilize the truth table listed on the 10 column (O_{10} to O_1) form. The eight output devices should use columns O_8 to O_1 leaving O_{10} and O_9 blank. Each truth table page accommodates up to 64 words.

Fill in the appropriate word number address for each word bit pattern and reproduce either form as required.

A High voltage level on data Out lines is defined as a H or a logic "0".
A Low voltage level on data Out lines is defined as a L or a logic "1".

Either Letters ("H" or "L") or Numbers ("1" or "0") may be used in the truth tables.

Punched Card Format

1st Card or Line (80 Columns Max): Enter Company Name – Part Number – Date – Number of "L's" In Pattern
(Free Form Entry No Commas)

CARD 1

COMPANY NAME CX1816 - 2052 7 - 12 - 70 L = 796

2nd Card Or Line thru Last (80 Columns Max)
ENTER WORD ADDRESS OF FIRST DATA FIELD IN COLUMNS 1 THRU 5

Enter First Data Field	($O_{10} - O_1$) In Columns 8 thru 17	or ($O_4 - O_1$) In Columns 14 thru 17
Enter Second Data Field	($O_{10} - O_1$) In Columns 19 thru 28	or ($O_4 - O_1$) In Columns 25 thru 28
Enter Third Data Field	($O_{10} - O_1$) In Columns 30 thru 39	or ($O_4 - O_1$) In Columns 36 thru 39
Enter Fourth Data Field	($O_{10} - O_1$) In Columns 41 thru 50	or ($O_4 - O_1$) In Columns 47 thru 50
Enter Fifth Data Field	($O_{10} - O_1$) In Columns 52 thru 61	or ($O_4 - O_1$) In Columns 58 thru 61
Enter Sixth Data Field	($O_{10} - O_1$) In Columns 63 thru 72	or ($O_4 - O_1$) In Columns 69 thru 72

CARD 2

00000 LLHHHLLHHH HHHHHHHHHH LLLLLLLLLH LHHHHHHHLL LLLLHHHHHL LLLLLLLLLL O_1

WORD ADDRESS OF

Note: Output 1(O_1) is always in cols. 17,28,39,50,61,72
Eight Output Devices use cols. 10–17 (O_8 - O_1) etc.
Four Output Devices use cols. 14–17 (O_4 - O_1) etc.

CARD 3

00006 LLLLLLLLLL HHHHHHHHHH LLLHHLLHHL LHHHHHLLLL LLLLHHHLHL HHHHHHHLHL

LAST CARD

01020 LLLLLLLLLL LLLHHHHHLL LLHHHHHLLL HHHHHLLLLL

CUSTOMER NAME ____

CUSTOMER PART NO. __________________________

A high voltage level on data out lines is defined as a "H" or a logic "0"

A low voltage level on data out lines is defined as a "L" or a logic "1"

Page ______ **of** ______

Word Number	OUTPUT					Word Number	OUTPUT					Word Number	OUTPUT					Word Number	OUTPUT				
	O_5	O_4	O_3	O_2	O_1		O_5	O_4	O_3	O_2	O_1		O_5	O_4	O_3	O_2	O_1		O_5	O_4	O_3	O_2	O_1

CUSTOMER NAME ____

CUSTOMER PART NO. ________________________

A high voltage level on data out lines is defined as a "H" or a logic "0"

A low voltage level on data out lines is defined as a "L" or a logic "1"

Page______of______

Word Number	OUTPUT										Word Number	OUTPUT									
	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1

PROM MMI FORMAT

MMI can program PROMS at our facility. You can elect to send us the truth tables in following format (listed below), to aid turn around time, the information can be sent directly to us by either TWX 910-339-9229 or via mail.

CUSTOMERS NAME: _____

PURCHASE ORDER NUMBER: _____

MMI PART NUMBER: _____

CUSTOMER SYMBOLIZED PART NUMBER: _____

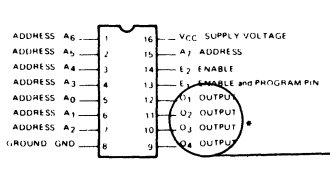
TRUTH TABLE NUMBER: _____

NUMBER OF TRUTH TABLES: _____

TOTAL NUMBER OF PARTS: _____

NUMBER OF PARTS OF EACH TRUTH TABLE: _____

(25 BELL CHARACTERS BEFORE START OF TRUTH TABLE)



START OF TAPE — END OF TAPE

BEGIN DATA FIELD

DATA FIELD (H = HIGH VOLTAGE, L = LOW)

FINISHED DATA FIELD

S B H H L H F — BHHHHF — BHLLHF — etc. — BHLLLFE

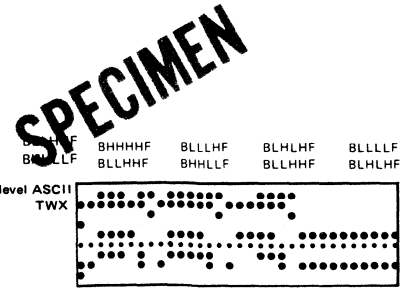
O_4 O_3 O_2 O_1

WORD 0 — WORD 1 — WORD 2 — WORD 31 OR 127 OR 255 OR 511

*For Eight Output Devices, the Format is 0_8 0_7 0_6 0_5 0_4 0_3 0_2 0_1

NOTE: ALL OTHER EXTRANEOUS CHARACTERS SUCH AS LINE FEED AND CARRIAGE RETURN ARE IGNORED

Sam Electronics
AAAAA1234
6300
897T
1225
3
3
1



**CHANNEL 1 MSB

2-4/10M/NR1

BIPOLAR CUSTOM CHARACTER GENERATOR ROMS (UP TO 128 CHARACTERS OF 9 x 9)

5297/6297 5299/6299

Monolithic Memories INCORPORATED

	MIL.	COM.	7 x 9 ROW SCAN	9 x 9 ROW OR COLUMN SCAN
5297	X		X	
6297		X	X	
5299	X			X
6299		X		X

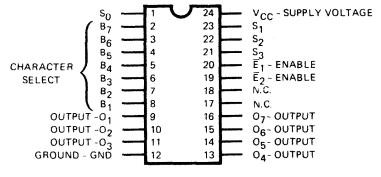
PRODUCT FEATURES

- Specifically Designed for Custom 7 x 9 Row Scan and 9 x 9 Font Character Generators
- 128 Characters in One Package
- Low Power Dissipation – 450mW
- Standard Packaging – 24 Pin Dip
- Single 5 Volt Supply
- 175 nsec Max. Access Time

APPLICATIONS

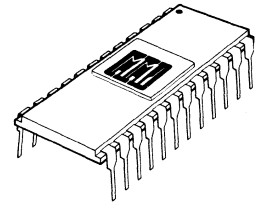
- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting
- Navigation Systems

PIN CONFIGURATION – 5297/6297 (7 x 9 Row Scan)

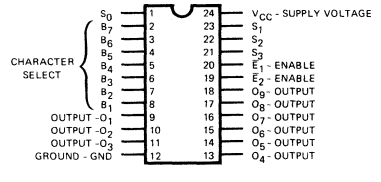


NOTE 1): S_0, S_1, S_2, S_3 are used for the character scan.
2): Both enables must be low to activate the device.

PACKAGE CONFIGURATION

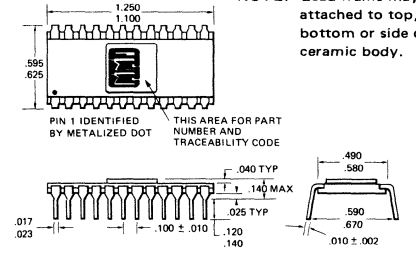


PIN CONFIGURATION 5299/6299 (9 x 9 Row or Column Scan)



NOTE 1): S_0, S_1, S_2, S_3 are used for the character scan.
2): Both enables must be low to activate the device.

PACKAGE OUTLINE



Monolithic Memories INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

JULY 1973

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.5 to 7 V
Input Voltage	-1.2 to 7.0 V
Output Current	100 mA
Storage Temperature	-65 to 160°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.

Functional operation at these limits is not guaranteed or implied.

D.C. CHARACTERISTICS* — Memory Outputs are Open Collector

PARAMETER		CONDITIONS	5297/5299 MIN.	5297/5299 TYP.[1]	5297/5299 MAX.	6297/6299 MIN.	6297/6299 TYP.[1]	6297/6299 MAX.	UNITS
I_F	Input Load Current, All inputs	V_{CC} = Max, V_F = 0.45 V			-250			-250	μA
I_R	Input Leakage Current, All inputs	V_{CC} = Max, V_R = 2.40 V			25			25	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 6 mA			0.50				V
		V_{CC} = Min, I_{OL} = 6 mA						0.50	V
I_{CC}	Power Supply Current	V_{CC} = 5.00 V, All inputs at 2.4 V		90	135		90	135	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4 V			100			100	μA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = -5.0 mA			-1.0			-1.0	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF

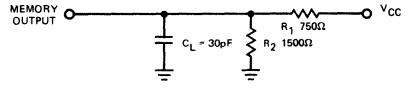
* Unless otherwise indicated, all limits for the 6297/6299 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5297/5299 are guaranteed for 5 V ±10% in a free air temperature of -55 to 125°C.

1. Typical values are measured at 5.0 V and 25°C.

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

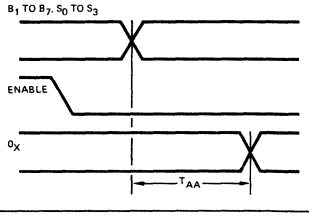
TEST	SYMBOL	CONDITIONS	5297/5299 TYP.	5297/5299 MAX.	6297/6299 TYP.	6297/6299 MAX.	UNITS
Access Time	T_{AA}		110	175	110	175	ns
Enable Recovery Time	T_{ER}	Word Addressed is Storing a low. See Fig 2.	20	60	20	60	ns
Enable Access Time	T_{EA}	Word Addressed is Storing a low. See Fig 2.	35	60	35	60	ns

STANDARD TEST LOAD



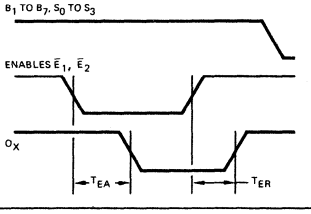
Input pulse amplitude = 2.5V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts.
Speed measurements are made at 1.4V
Output loading is 6mA and 30pF as given in std. load.

Fig. 1
ACCESS TIME



A_X = Any Address
O_X = Any Output

Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET RL = Pullup resistor value
N = The number of TTL loads the memroy must drive
M = The number of memory packages wire OR'ed
I_{oL} = 6 mA for the 5297/6297
6 mA for the 5299/6299
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Two 6299 memory packages are wire OR'ed and 2 Series 74 TTL gates must be driven find the range of permissible pull-up resistors at V_{CC} = 5.0 V.

M = 2
N = 2
I_F = 1.6 mA
I_R = 40 μA
I_{oL} = 15 mA

$$R_L(\text{max}) = \frac{V_{CC}-2.40\ V}{M(100\mu A)+N(I_R)} \qquad R_L(\text{max}) = \frac{5.0-2.4\ V}{2(100\mu A)+2(40\mu A)} = 9286\ \text{ohms}$$

$$R_L(\text{min}) = \frac{V_{CC}-0.45\ V}{I_{OL}-N(I_F)} \qquad R_L(\text{min}) = \frac{5.0-0.45\ V}{6\ mA-2(1.6\ mA)} = 1625\ \text{ohms}$$

DESCRIPTION

A 7 x 9 font row scan character has 7 outputs and 9 rows per character. The character is formed one row at a time. 9 words of a ROM with 7 outputs per word are required for each character. 128 characters required on 1152 x 7 ROM which is the size of the 5297/6297. For custom column scan 7 x 9 characters consult the 6073 data sheet.

A 9 x 9 font character has 9 outputs and 9 rows of columns per character depending upon whether we are forming a row or column scan. 9 words of a ROM with 9 outputs per row are required for each character. 128 characters require an 1152 x 9 ROM which is the 5299/6299.

S_3, S_2, S_1, and S_0 pins are used to scan through the 9 ROM words per character. This is usually implemented by "short counting" a 4 bit binary counter so that it counts from 0000 to 1000 (9 counts) continuously (See applications section). B_1 thru B_7 are used to pick one of the 128 characters. B_1 is the least significant binary digit and B_7 is the most significant binary digit.

The memory outputs are open collector and pullup resistors are required. The enable E_1, and E_2 must both be low to activate the part. A disabled part (E_1 or E_2 high) has high memory outputs permitting wire ORing or blanking.

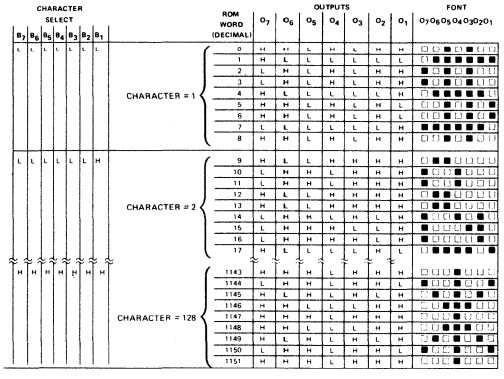
CUSTOM FONT

It's easy to go from custom font to the punched card or tape format preferred by Monolithic Memories Inc. Several examples are shown. We have arbitarily assumed that a character is formed by a series of low memory outputs in a background of high memory outputs. This assumption, of course can be reversed.

EXAMPLE – CUSTOM TRUTH TABLE CODING – (5297/6297)

7 x 9 ROW SCAN

The characters **$**, &, *, are shown below along with the ROM coding. A "filled in" dot is arbitarily coded with a low (L)



USE OF CUSTOM TRUTH TABLE FORM – 5297/6297

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 7 x 9 Row Scan example:

WORD NUMBER	PIN	16	15	14	13	11	10	9
		OUTPUTS						
		O_7	O_6	O_5	O_4	O_3	O_2	O_1
0		H	H	L	H	L	H	H
1		H	L	L	L	L	L	L
•		•	•	•	•	•	•	•
•		•	•	•	•	•	•	•
•		•	•	•	•	•	•	•
1151		H	H	H	L	H	H	H

NOTE:

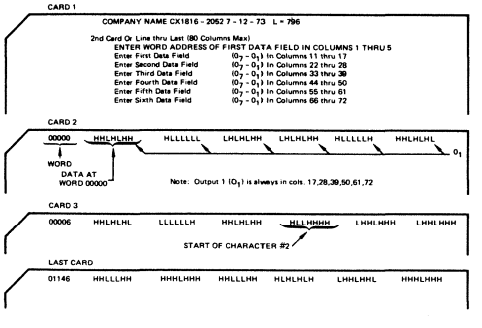
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.

PUNCHED CARD OR TAPE FORMAT – 5297/6297

The cards below are coded with the 7 x 9 row scan example.

Punched Card Or Tape Format

1st Card or Line (80 Columns Max): Enter Company Name – Part Number – Date – Number of "L's" In Pattern (Free Form Entry No Commas) (Paper Tape Format. Terminates each Line with Carriage Return and Linefeed)



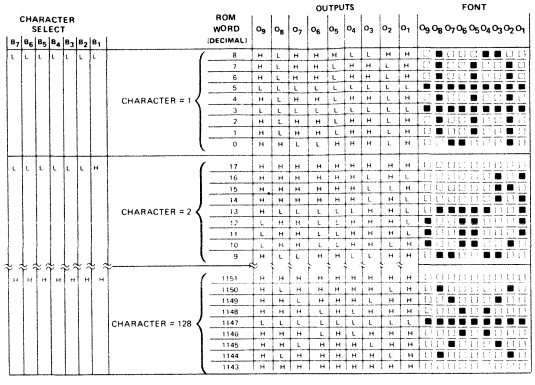
NOTE:

Leading edge zeroes in the word number may be eliminated. Columns 73 thru 80 are for comments.

EXAMPLE – CUSTOM TRUTH TABLE CODING – (5299/6299)

9 x 9 COLUMN SCAN

The characters $, &, *, can be seen in the font if this page is rotated 90° clockwise. A "filled in" dot is abritarily coded with a low (L).



9 x 9 ROW SCAN

The 9 x 9 row scan translation would be similar to the 7 x 9 row scan previously shown except that there would be a 9 x 9 font for each character and outputs 8 and 9 in the ROM would be used and coded.

USE OF CUSTOM TRUTH TABLE FORM – 5299/6299

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is show below coded to the 9 x 9 column scan example:

WORD NUMBER	PIN	18	17	16	15	14	13	11	10	9
		OUTPUTS								
		O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0		H	H	L	L	H	H	H	L	H
1		H	L	H	H	L	H	H	L	H
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
1151		H	H	H	H	H	H	H	H	H

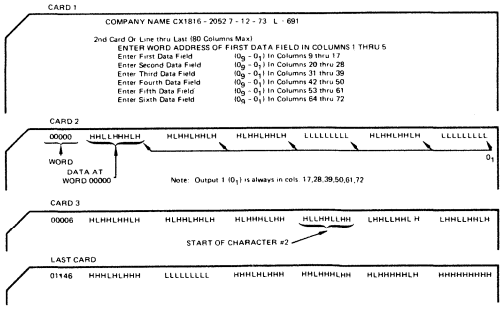
NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.

PUNCHED CARD OR TAPE FORMAT

The cards below are coded with the 9 x 9 column scan example.

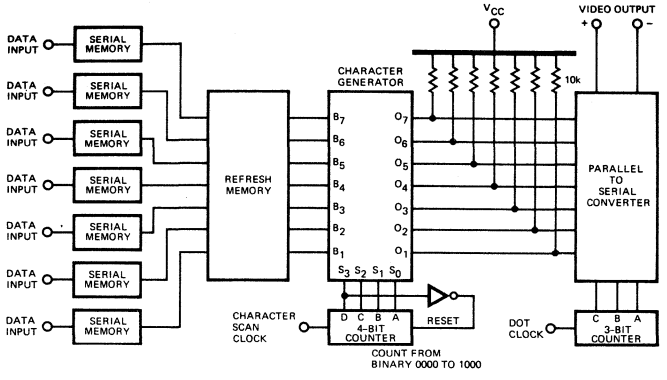
Punched Card Or Tape Format

1st Card or Line (80 Columns Max): Enter Company Name – Part Number – Date – Number of "L's". In Pattern (Free Form Entry No Commas) (Paper Tape Format, Terminate each Line with Carriage Return and Linefeed)

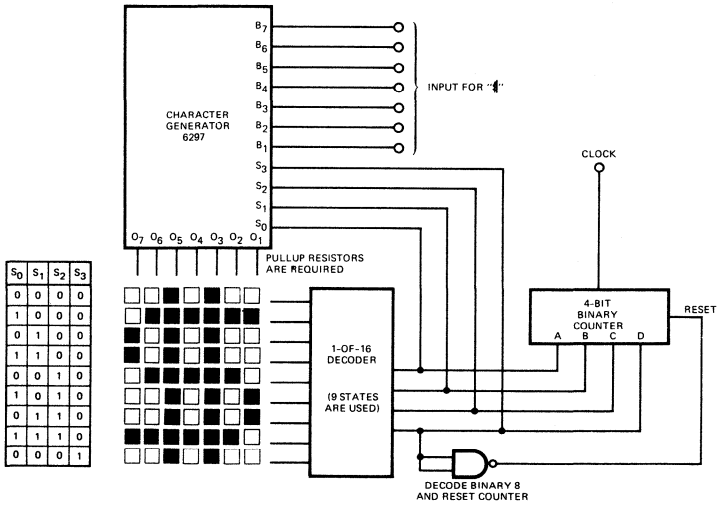


NOTE:
Leading edge zeroes in the word number may be eliminated. Columns 73 thru 80 are for comments.

CRT CHARACTER DISPLAY BLOCK DIAGRAM



GENERATION OF THE CHARACTER "$" IN A 7 x 9 ROW SCAN



S_0	S_1	S_2	S_3
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1

HIGH PERFORMANCE BIPOLAR 5×7 CHARACTER GENERATOR (ROW SCAN)

MM6055

USASCII 64 CHARACTERS

Monolithic Memories
INCORPORATED

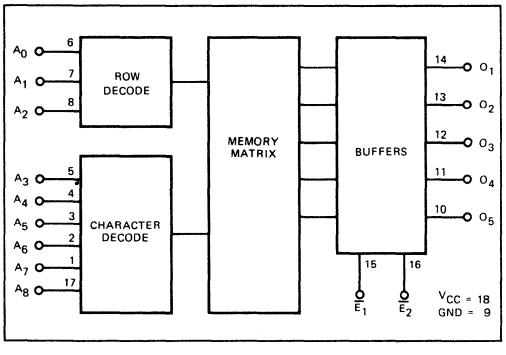
PRODUCT FEATURES:

- Speed 10 MHz
- Low Power Dissipation – 450 mW
- Standard Packaging – 18 Pin Dip
- Single 5 Volt Supply
- 100 ns Max. Access Time
- 64 Characters in One Package

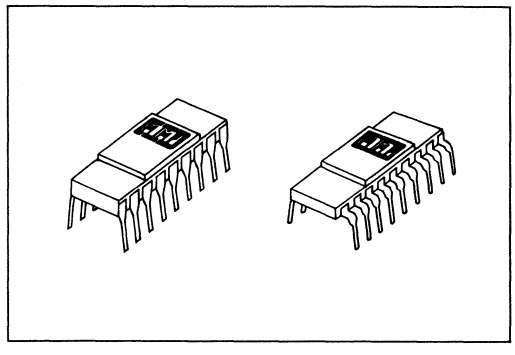
APPLICATIONS

- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting

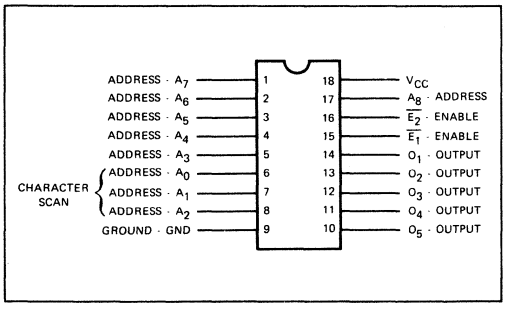
BLOCK DIAGRAM



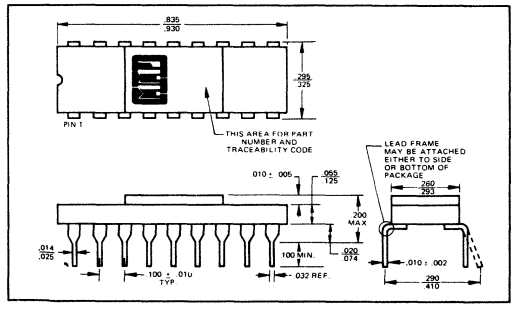
PACKAGE CONFIGURATION



PIN CONFIGURATION



PACKAGE OUTLINE



Monolithic Memories
INCORPORATED

1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

SEPTEMBER 1972

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7v
Input Current	20ma
Output Current	100ma
Ambient Temperature	−65° to +125°C
Storage Temperature	−65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range, T_A	MM6055	0° to 75°C
Supply Voltage	MM6055	Max 5.25v; Min 475v

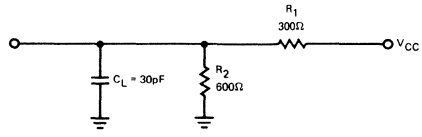
ELECTRICAL CHARACTERISTICS * Memory outputs are open collector.

		MM6055			
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
I_{FA} – Address Input Load Current	V_{CC} = Max; V_A = 0.4v		−1.0	−1.6	ma
I_{FE} – Enable Input Load Current	V_{CC} = Max; V_E = 0.4v		−1.0	−1.6	ma
I_{RA} – Address Input Leakage Current	V_{CC} = Max; V_A = 2.4v			40	μa
I_{RE} – Enable Input Leakage Current	V_{CC} = Max; V_E = 2.4v			40	μa
V_{OL} – Low Level Output Voltage	V_{CC} = Min; I_{OL} = 8ma		0.25	0.45	v
I_{CC} – Power Supply Current	V_{CC} = 5.0v		90	125	ma
V_{IL} – Low Level Input Voltage				0.85	v
V_{IH} – High Level Input Voltage		2.0			v
I_{CEX} – Output Leakage Current	V_{CC} = Max; V_{CEX} = Max			250	μa
V_{IC} – Input Clamp Voltage	V_{CC} = Min; I_I = −10ma			−1.5	v
BV_I – Input Breakdown Voltage	V_{CC} = Max; I_I = 1.0ma	5.5			v
C_I – Input Capacitance	V_{CC} = 5.0v; V_I = 2.0v		5.0		pf
C_O – Output Capacitance	V_{CC} = 5.0v; V_O = 2.0v Output in "O" state		7.0		pf

*All limits apply for 5V ±5%, 0°C to 75°C

SWITCHING TEST CIRCUITS

STANDARD TEST LOAD



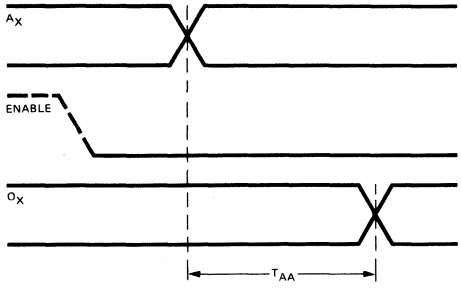
Input pulse amplitude = 2.5v
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4v
Output loading is 15ma and 30pf as given in std. load at right

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0 V, Std. Load)

TEST	SYMBOL	CONDITIONS	MM6055		UNITS
			TYP.	MAX.	
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	50	100	ns
Enable Access Time	T_{EA}	Word Addressed is Storing a low See Fig. 2	38	50	ns
Enable Recovery Time	T_{ER}	Word Addressed is Storing a low See Fig. 2	20	50	ns

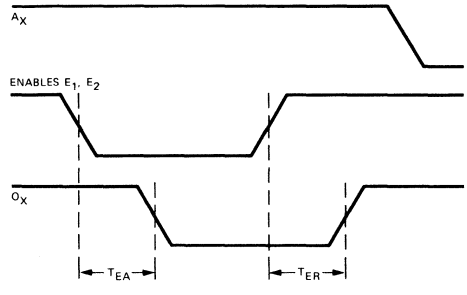
TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

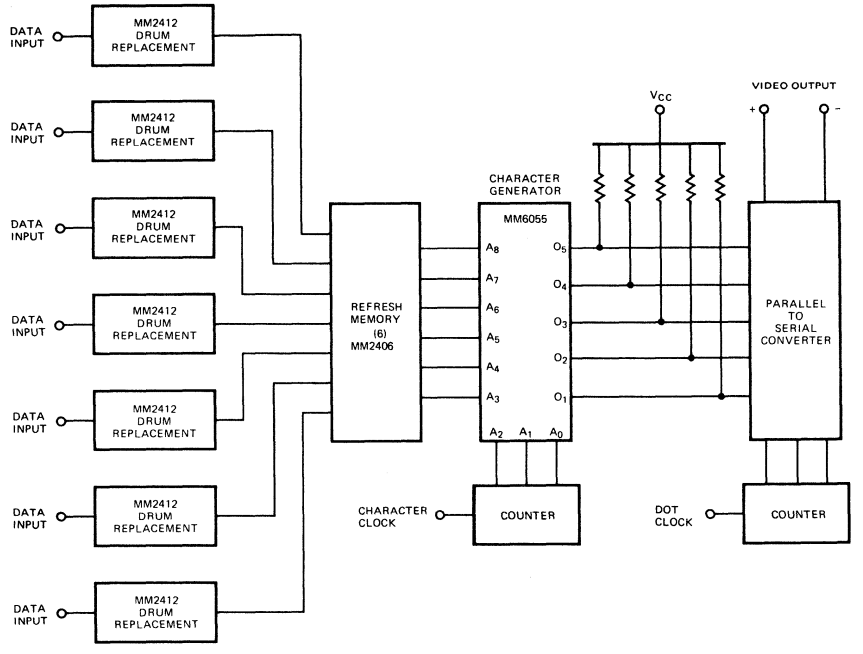


AX = Any Address
OX = Any Output

Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



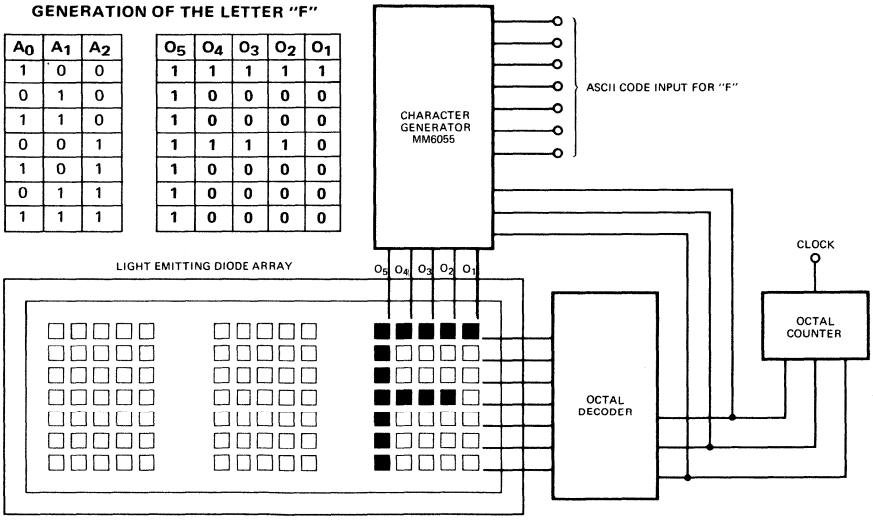
CRT CHARACTER DISPLAY BLOCK DIAGRAM



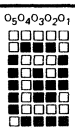
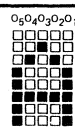
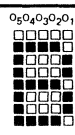
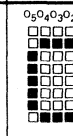
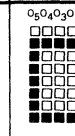
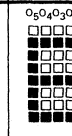
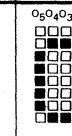
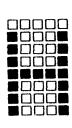
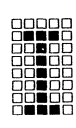
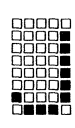
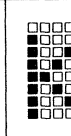
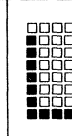
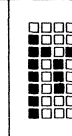
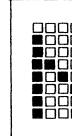
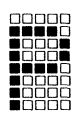
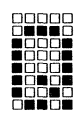
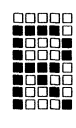
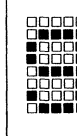
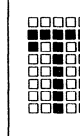
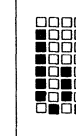
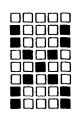
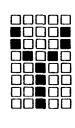
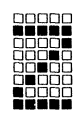
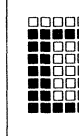
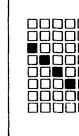
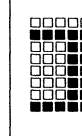
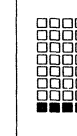
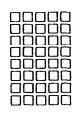
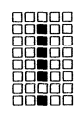
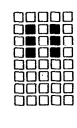
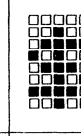
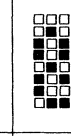
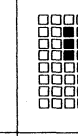
GENERATION OF THE LETTER "F"

A_0	A_1	A_2
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1

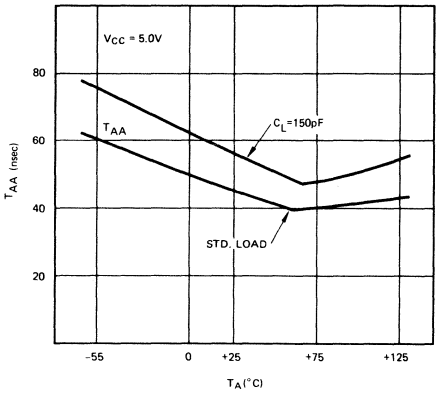
O_5	O_4	O_3	O_2	O_1
1	1	1	1	1
1	0	0	0	0
1	0	0	0	0
1	1	1	1	0
1	0	0	0	0
1	0	0	0	0
1	0	0	0	0

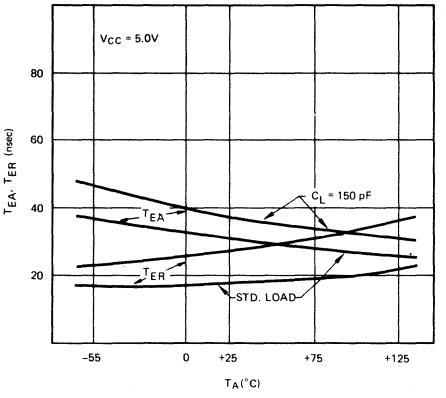


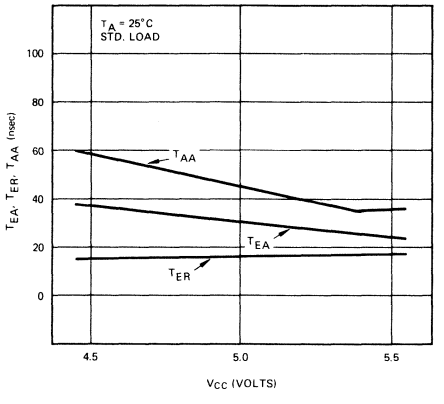
A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

ASCII INPUT ADDRESS	B_1 B_2 B_3 A_3 A_4 A_5 000	A_3 A_4 A_5 100	A_3 A_4 A_5 010	A_3 A_4 A_5 110	A_3 A_4 A_5 001	A_3 A_4 A_5 101	A_3 A_4 A_5 011	A_3 A_4 A_5 111
B_4 B_5 B_6* A_6 A_7 A_8 000	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 
A_6 A_7 A_8 100								
A_6 A_7 A_8 010								
A_6 A_7 A_8 110								
A_6 A_7 A_8 001								
A_6 A_7 A_8 101								
A_6 A_7 A_8 011								
A_6 A_7 A_8 111								

*FROM THE USASCII CODE $A_8=B_7=\overline{B_6}$







CHARACTER GENERATOR OPERATION

The intended application for the MM6055 is the generation of 64 USACII characters utilizing a readout system which generates the characters horizontally a 5 bit line at a time. Each 35 bit character is composed of 7 distinct 5 bit lines. One of the 64 characters is selected by the 6 bit address applied to A_3 thru A_8. The particular 5 bit line within each character is determined by the 3 bit address applied to A_0, A_1 and A_2. The binary address 000 on A_0, A_1 and A_2 provides a blank line for character line spacing. The memory is enabled when both E_1 and E_2 are low (logic "0").

HIGH PERFORMANCE BIPOLAR 5×7 CHARACTER GENERATOR (COLUMN SCAN)

MM6056

USASCII 64 ALPHA-NUMERICS

Monolithic Memories
INCORPORATED

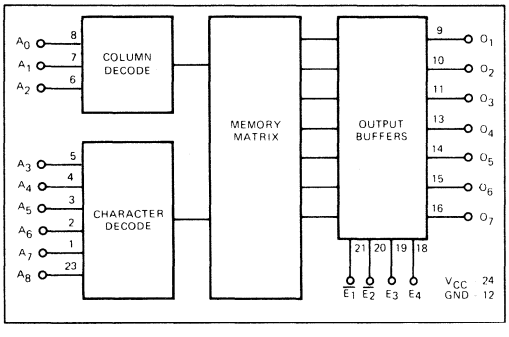
PRODUCT FEATURES:

- 64 Characters in One Package
- Low Power Dissipation – 450mW
- Standard Packaging – 24 Pin Dip
- Single 5 Volt Supply
- 175 nsec Max. Access Time

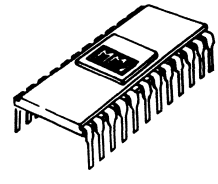
APPLICATIONS:

- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting

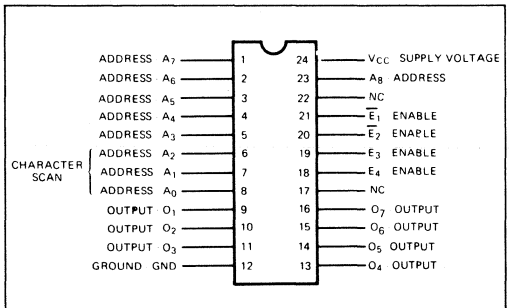
BLOCK DIAGRAM



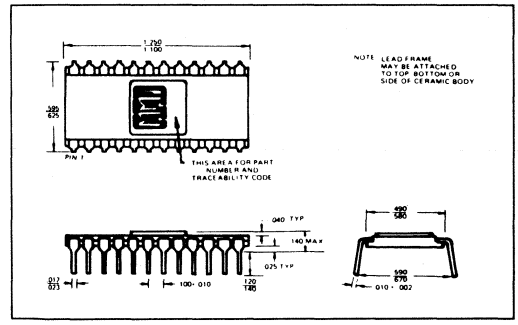
PACKAGE CONFIGURATION



PIN CONFIGURATION



PACKAGE OUTLINE



Monolithic Memories
INCORPORATED

1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

SEPTEMBER 1972

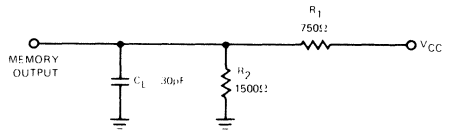
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Current	20mA
Output Current	100mA
Ambient Temperature	−65 to +125 C
Storage Temperature	−65 to +150 C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range, T_A	0 to 75 C
Supply Voltage	Max. 5.25V; Min. 4.75V

STANDARD TEST LOAD



Input pulse amplitude = 2.5V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4V
Output loading is 6mA and 30pF as given in std. load

*ELECTRICAL CHARACTERISTICS Memory outputs are open collector

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
I_{FA}	Address Input Load Current	V_{CC} = 5.25V	V_A = 0.4V		−80	−250	μA
I_{FE}	Enable Input Load Current	V_{CC} = 5.25V	V_E = 0.4V		−80	−250	μA
I_{RA}	Address Input Leakage Current	V_{CC} = 5.25V	V_A = 2.4V			40	μA
I_{RE}	Enable Input Leakage Current	V_{CC} = 5.25V	V_E = 2.4V			40	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V	I_{OL} = 6mA		0.3	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0V			90	135	mA
V_{IL}	Low Level Input Voltage					0.8	V
V_{IH}	High Level Input Voltage			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = 5.25V	V_{CEX} = V_{CC} V			250	μA
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V	I_I = −5mA			−1.0	V
BV_I	Input Breakdown Voltage	V_{CC} = 5.25V	I_I = 1.0mA	5.5			V
C_I	Input Capacitance	V_{CC} = 5.0V	V_I = 2.0V		5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V	V_O = 2.0V		7.0		pF
		Output in High State					

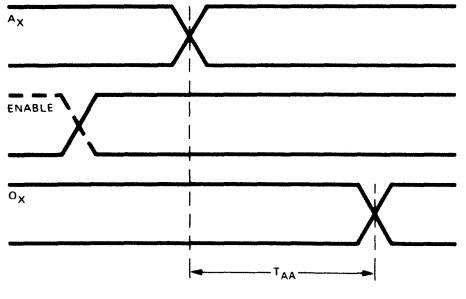
*All limits apply for 5V ±5%, 0°C to 75°C

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

TEST	SYMBOL	CONDITIONS	TYP.	MAX.	UNITS
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	70	175	nsec
Enable Access Time	T_{EA}	Word Addressed is Storing a Low See Fig. 2	45	60	nsec
Enable Recovery Time	T_{ER}	Word Addressed is Storing a Low See Fig. 2	20	30	nsec

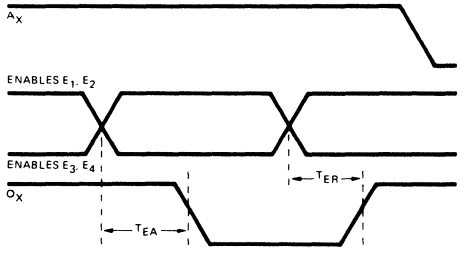
TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

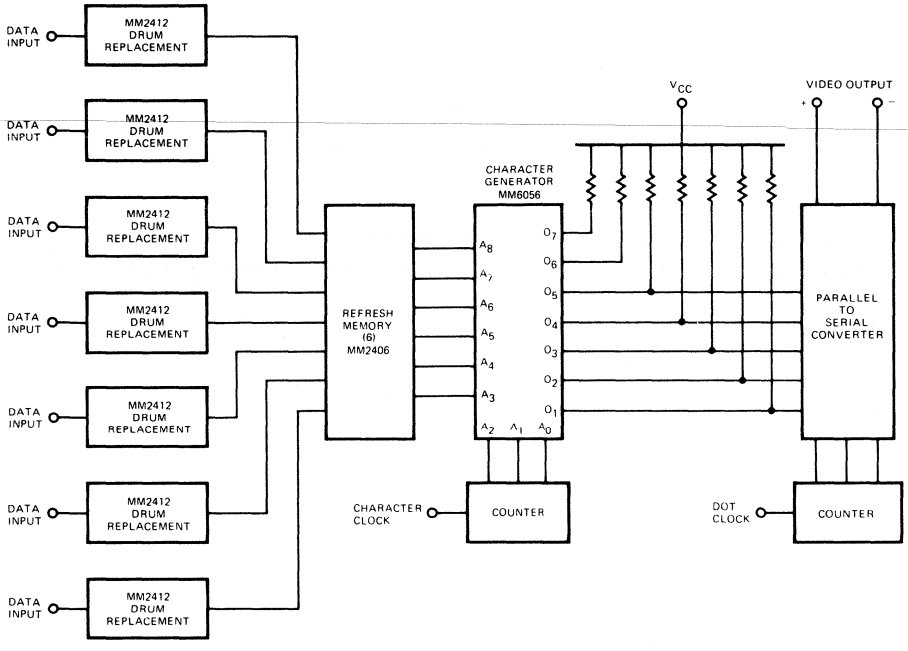


AX = Any Address
OX = Any Output

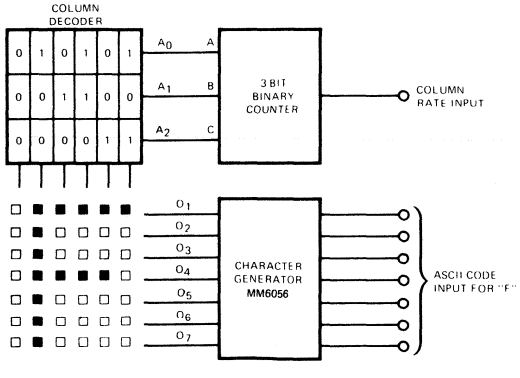
Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



CRT CHARACTER DISPLAY BLOCK DIAGRAM



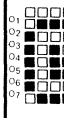
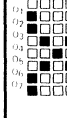
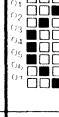
GENERATION OF THE LETTER "F"



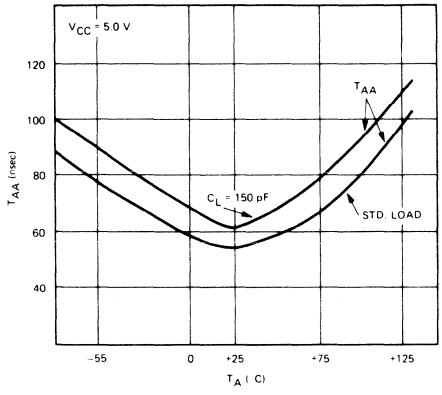
5 X 7 CHARACTER FONT*

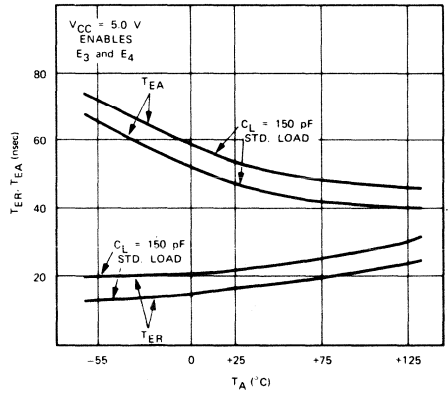
MM6056

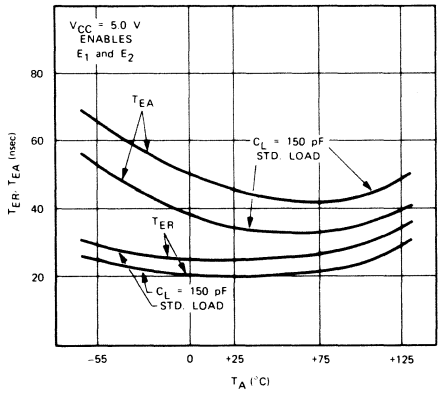
A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

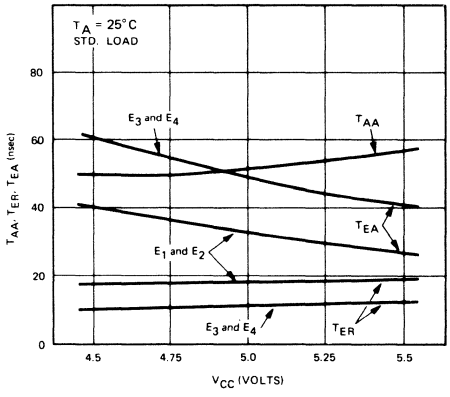
ASCII INPUT ADDRESS	$A_3\ A_4\ A_5$ 000	$A_3\ A_4\ A_5$ 100	$A_3\ A_4\ A_5$ 010	$A_3\ A_4\ A_5$ 110	$A_3\ A_4\ A_5$ 001	$A_3\ A_4\ A_5$ 101	$A_3\ A_4\ A_5$ 011	$A_3\ A_4\ A_5$ 111
$A_6\ A_7\ A_8$ 000								
$A_6\ A_7\ A_8$ 100								
$A_6\ A_7\ A_8$ 010								
$A_6\ A_7\ A_8$ 110								
$A_6\ A_7\ A_8$ 001								
$A_6\ A_7\ A_8$ 101								
$A_6\ A_7\ A_8$ 011								
$A_6\ A_7\ A_8$ 111								

* From the USASCII Code $A_8 = B_7 = \overline{B_6}$.









CHARACTER GENERATOR OPERATION

The intended application for the MM6056 is the generation of 64 USACII characters utilizing a readout system which generates the characters vertically a 7 bit line at a time. Each 35 bit character is composed of 7 distinct 5 bit lines. One of the 64 characters is selected by the 6 bit address applied to A_3 thru A_8. The particular 5 bit line within each character is determined by the 3 bit address applied to A_0, A_1 and A_2. The binary address 000 on A_0, A_1 and A_2 provides a blank line for character line spacing. The memory is enabled when either E_1 and E_2 are low (logic "0") or E_3 and E_4 are high (logic "1").

Monolithic
Memories
INCORPORATED

4-4/5M/N

HIGH PERFORMANCE BIPOLAR 5×7 CHARACTER GENERATOR (ROW SCAN)

MM6061

USASCII 128 CHARACTERS

Monolithic Memories
INCORPORATED

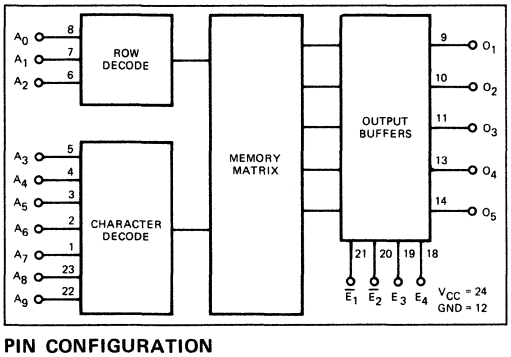
PRODUCT FEATURES:

- 128 Characters in One Package
- Low Power Dissipation – 450mW
- Standard Packaging – 24 Pin Dip
- Single 5 Volt Supply
- 175 nsec Max. Access Time

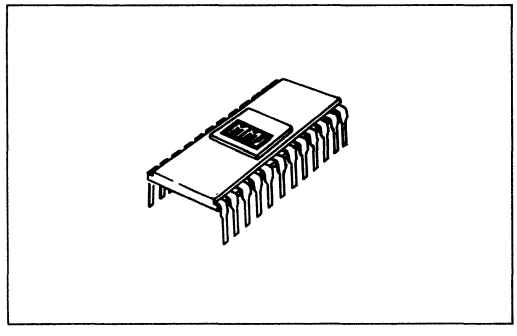
APPLICATIONS:

- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting

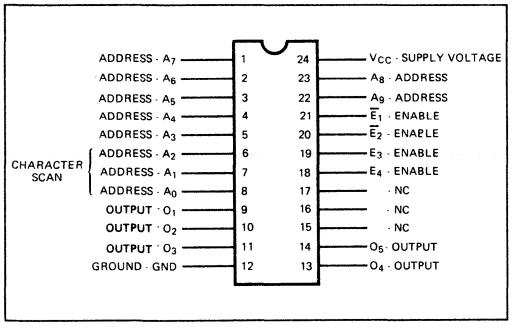
BLOCK DIAGRAM



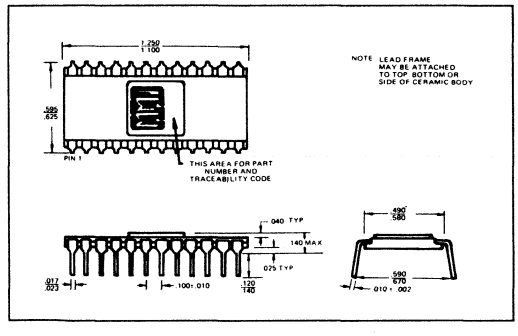
PACKAGE CONFIGURATION



PIN CONFIGURATION



PACKAGE OUTLINE



Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

SEPTEMBER 1972

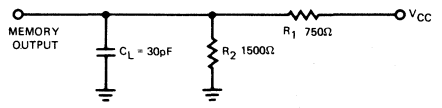
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Current	20mA
Output Current	100mA
Ambient Temperature	−65° to +125°C
Storage Temperature	−65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range, T_A	0° to 75°C
Supply Voltage	Max. 5.25V; Min. 4.75V

STANDARD TEST LOAD



Input pulse amplitude = 2.5V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4V
Output loading is 6mA and 30pF as given in std. load

*ELECTRICAL CHARACTERISTICS Memory outputs are open collector

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
I_{FA}	Address Input Load Current	V_{CC} = 5.25V	V_A = 0.4V		−80	−250	μA
I_{FE}	Enable Input Load Current	V_{CC} = 5.25V	V_E = 0.4V		−80	−250	μA
I_{RA}	Address Input Leakage Current	V_{CC} = 5.25V	V_A = 2.4V			40	μA
I_{RE}	Enable Input Leakage Current	V_{CC} = 5.25V	V_E = 2.4V			40	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V	I_{OL} = 6mA		0.3	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0V			90	135	mA
V_{IL}	Low Level Input Voltage					0.8	V
V_{IH}	High Level Input Voltage			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = 5.25V	V_{CEX} = V_{CC} V			250	μA
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V	I_I = −5mA			−1.0	V
BV_I	Input Breakdown Voltage	V_{CC} = 5.25V	I_I = 1.0mA	5.5			V
C_I	Input Capacitance	V_{CC} = 5.0V	V_I = 2.0V		5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V	V_O = 2.0V		7.0		pF
		Output in High State					

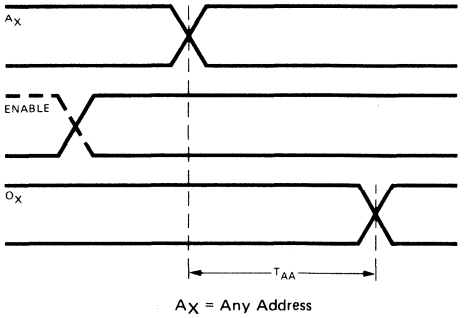
*All limits apply for 5V ± 5%, 0°C to 75°C

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

TEST	SYMBOL	CONDITIONS	TYP.	MAX.	UNITS
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	70	175	nsec
Enable Access Time	T_{EA}	Word Addressed is Storing a Low See Fig. 2	45	60	nsec
Enable Recovery Time	T_{ER}	Word Addressed is Storing a Low See Fig. 2	20	30	nsec

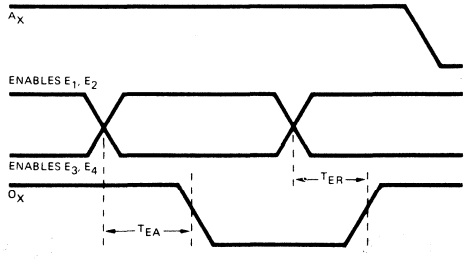
TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

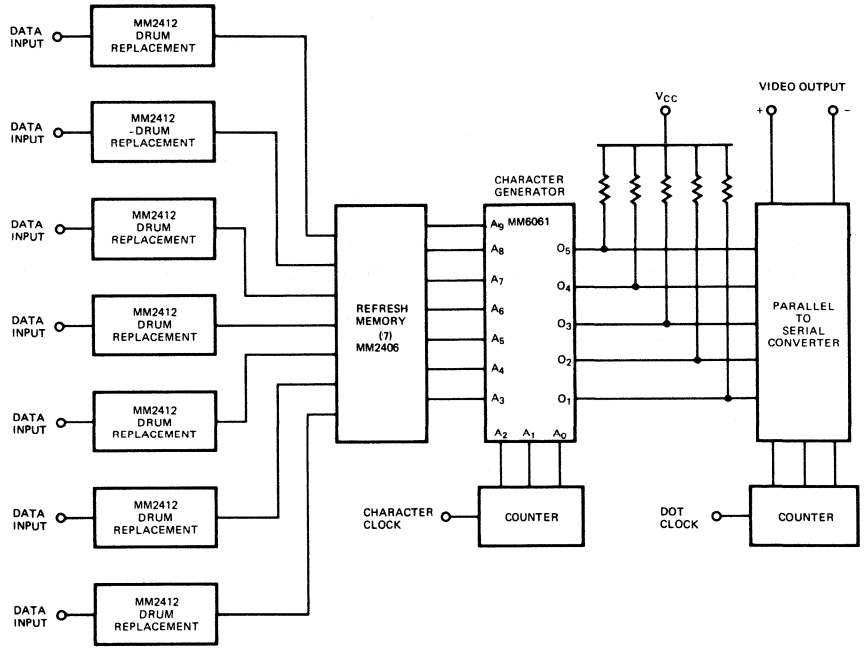


A_X = Any Address
O_X = Any Output

Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



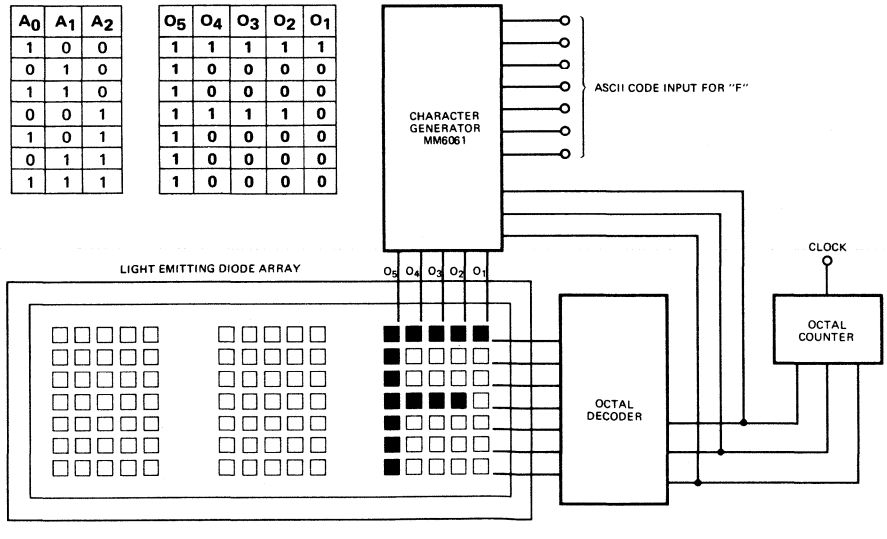
CRT CHARACTER DISPLAY BLOCK DIAGRAM



GENERATION OF THE LETTER "F"

A_0	A_1	A_2
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1

O_5	O_4	O_3	O_2	O_1
1	1	1	1	1
1	0	0	0	0
1	0	0	0	0
1	1	1	1	0
1	0	0	0	0
1	0	0	0	0
1	0	0	0	0



A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

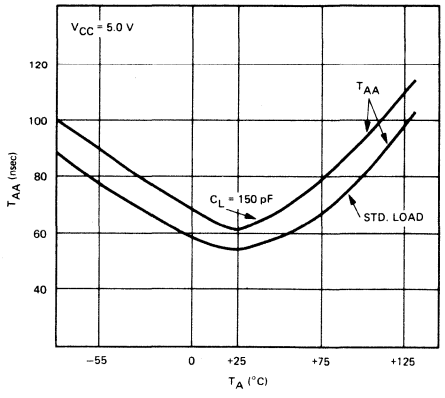
ASCII INPUT ADDRESS	$B_7B_6B_5$ $A_9A_8A_7$ 000 $O_5O_4O_3O_2O_1$	$A_9A_8A_7$ 001	$A_9A_8A_7$ 010	$A_9A_8A_7$ 011	$A_9A_8A_7$ 100	$A_9A_8A_7$ 101	$A_9A_8A_7$ 110	$A_9A_8A_7$ 111
$B_4B_3B_2B_1$ $A_6A_5A_4A_3$ 0000	(NUL)*	(DLE)*						
$A_6A_5A_4A_3$ 0001	(SOH)*	(DC1)*						
$A_6A_5A_4A_3$ 0010		(DC2)*						
$A_6A_5A_4A_3$ 0011	(ETX)*	(DC3)*						
$A_6A_5A_4A_3$ 0100	(EOT)*	(DC4)*						
$A_6A_5A_4A_3$ 0101	(ENQ)*	(NAK)*						
$A_6A_5A_4A_3$ 0110	(ACK)*	(SYN)*						
$A_6A_5A_4A_3$ 0111	(BEL)*	(ETB)*						

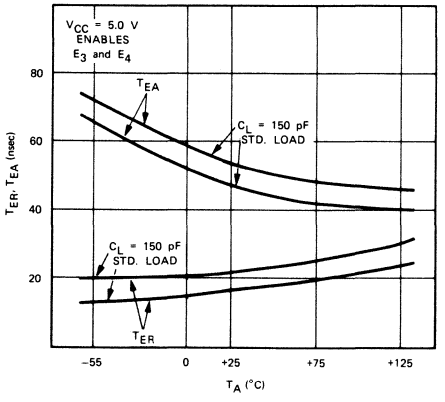
*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

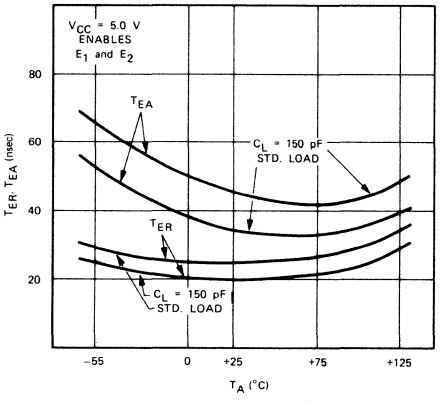
A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

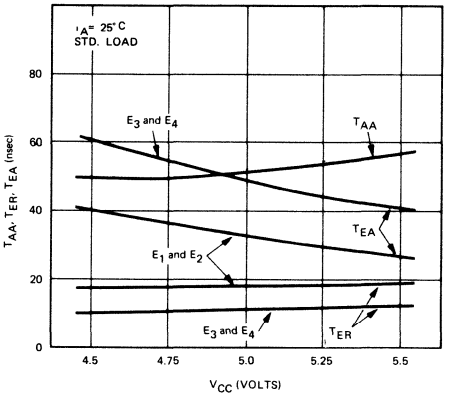
ASCII INPUT ADDRESS	$B_7B_6B_5$ $A_9A_8A_7$ 000 $O_5O_4O_3O_2O_1$	$A_9A_8A_7$ 001	$A_9A_8A_7$ 010	$A_9A_8A_7$ 011	$A_9A_8A_7$ 100	$A_9A_8A_7$ 101	$A_9A_8A_7$ 110	$A_9A_8A_7$ 111
$B_4B_3B_2B_1$ $A_6A_5A_4A_3$ 1000	(BS)*	(CAN)*						
$A_6A_5A_4A_3$ 1001	(HT)*	(EM)*						
$A_6A_5A_4A_3$ 1010	(LF)*	(SUB)*						
$A_6A_5A_4A_3$ 1011	(VT)*	(ESC)*						
$A_6A_5A_4A_3$ 1100	(FF)*	(FS)*						
$A_6A_5A_4A_3$ 1101	(CR)*	(GS)*						
$A_6A_5A_4A_3$ 1110	(SO)*	(RS)*						
$A_6A_5A_4A_3$ 1111	(SI)*	(US)*						(DEL)*

*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.









CHARACTER GENERATOR OPERATION

The intended application for the MM6061 is the generation of 128 USACII characters utilizing a readout system which generates the characters horizontally a 5 bit line at a time. Each 35 bit character is composed of 7 distinct 5 bit lines. One of the 128 characters is selected by the 7 bit address applied to A_3 thru A_9. The particular 5 bit line within each character is determined by the 3 bit address applied to A_0, A_1 and A_2. The binary address 000 on A_0, A_1 and A_2 provides a blank line for character line spacing. The memory is enabled when either E_1 and E_2 are low (logic "0") or E_3 and E_4 are high (logic "1").

HIGH PERFORMANCE BIPOLAR 5×7 CHARACTER GENERATOR (COLUMN SCAN)

MM6062

USASCII 128 CHARACTERS

Monolithic Memories
INCORPORATED

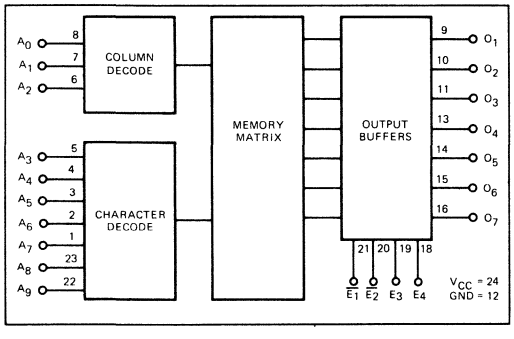
PRODUCT FEATURES:

- 128 Characters in One Package
- Low Power Dissipation – 450mW
- Standard Packaging – 24 Pin Dip
- Single 5 Volt Supply
- 175 nsec Max. Access Time

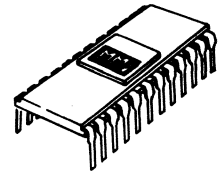
APPLICATIONS:

- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting

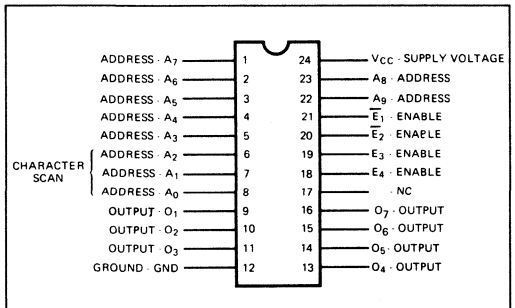
BLOCK DIAGRAM



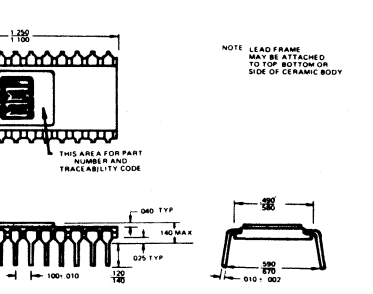
PACKAGE CONFIGURATION



PIN CONFIGURATION



PACKAGE OUTLINE



Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

JUNE 1972

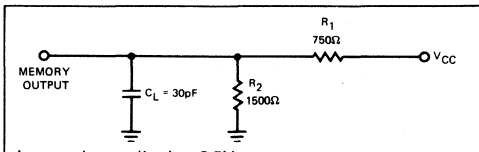
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Current	20mA
Output Current	100mA
Ambient Temperature	−65° to +125°C
Storage Temperature	−65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range, T_A	0° to 75°C
Supply Voltage	Max. 5.25V; Min. 4.75V

STANDARD TEST LOAD



Input pulse amplitude = 2.5V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4V
Output loading is 6mA and 30pF as given in std. load

*ELECTRICAL CHARACTERISTICS Memory outputs are open collector

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
I_{FA}	Address Input Load Current	V_{CC} = 5.25V	V_A = 0.4V		−80	−250	μA
I_{FE}	Enable Input Load Current	V_{CC} = 5.25V	V_E = 0.4V		−80	−250	μA
I_{RA}	Address Input Leakage Current	V_{CC} = 5.25V	V_A = 2.4V			40	μA
I_{RE}	Enable Input Leakage Current	V_{CC} = 5.25V	V_E = 2.4V			40	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V	I_{OL} = 6mA		0.3	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0V			90	135	mA
V_{IL}	Low Level Input Voltage					0.8	V
V_{IH}	High Level Input Voltage			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = 5.25V	V_{CEX} = V_{CC} V			250	μA
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V	I_I = −5mA			−1.0	V
BV_I	Input Breakdown Voltage	V_{CC} = 5.25V	I_I = 1.0mA	5.5			V
C_I	Input Capacitance	V_{CC} = 5.0V	V_I = 2.0V		5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V	V_O = 2.0V		7.0		pF
		Output in High State					

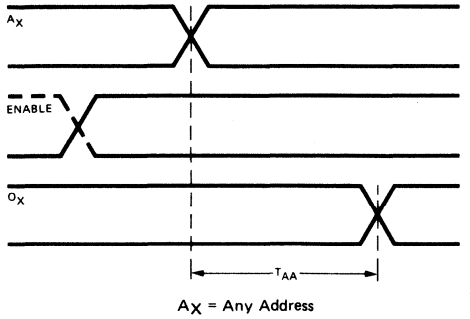
*All limits apply for 5V ±5%, 0°C to 75°C

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

TEST	SYMBOL	CONDITIONS	TYP.	MAX.	UNITS
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	70	175	nsec
Enable Access Time	T_{EA}	Word Addressed is Storing a Low See Fig. 2	45	60	nsec
Enable Recovery Time	T_{ER}	Word Addressed is Storing a Low See Fig. 2	20	30	nsec

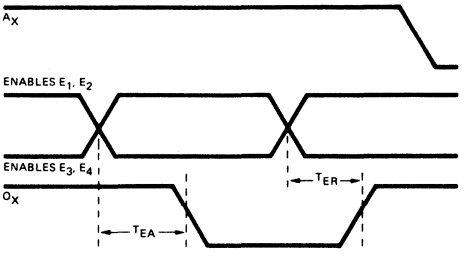
TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

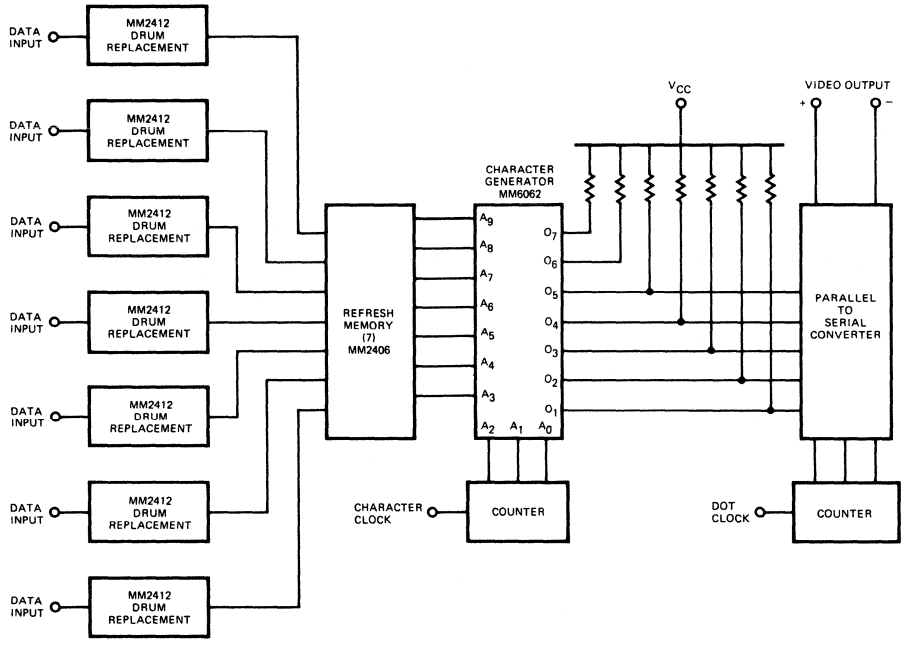


A_X = Any Address
O_X = Any Output

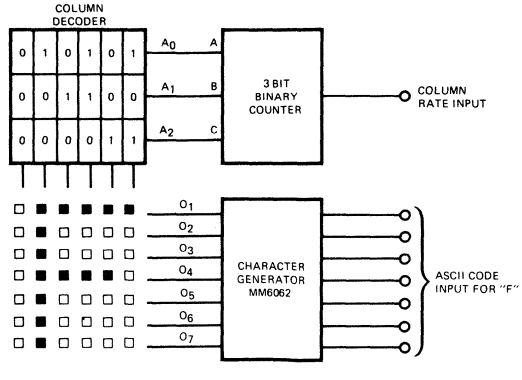
Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



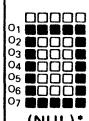
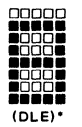
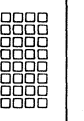
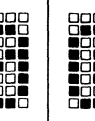
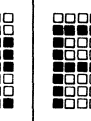
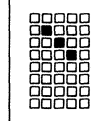
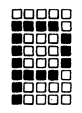
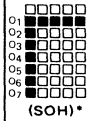
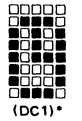
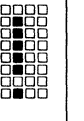
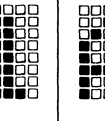
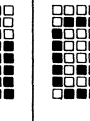
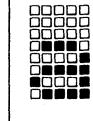
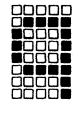
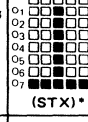
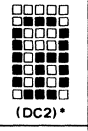
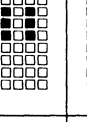
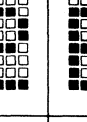
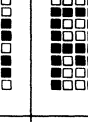
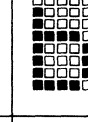
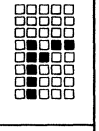
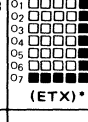
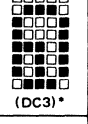
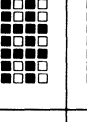
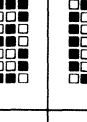
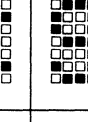
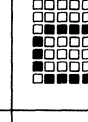
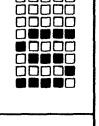
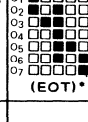
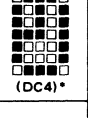
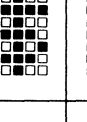
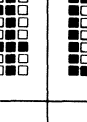
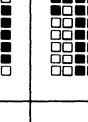
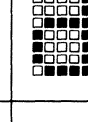
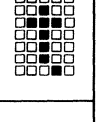
CRT CHARACTER DISPLAY BLOCK DIAGRAM



GENERATION OF THE LETTER "F"

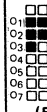
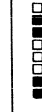
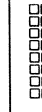
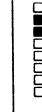
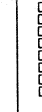
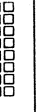
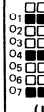
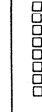
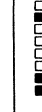
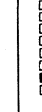
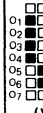
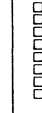
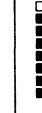
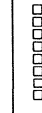
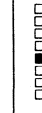
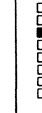
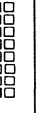


A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

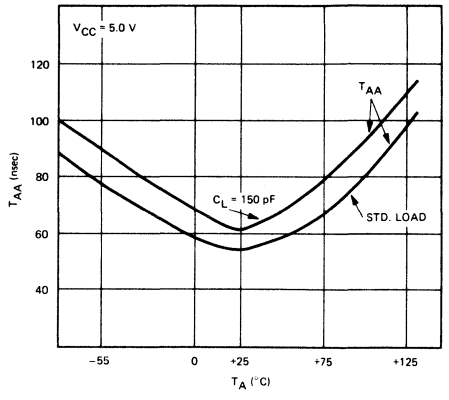
ASCII INPUT ADDRESS	$B_7B_6B_5$ $A_9A_8A_7$ 000	$A_9A_8A_7$ 001	$A_9A_8A_7$ 010	$A_9A_8A_7$ 011	$A_9A_8A_7$ 100	$A_9A_8A_7$ 101	$A_9A_8A_7$ 110	$A_9A_8A_7$ 111
$B_4B_3B_2B_1$ $A_6A_5A_4A_3$ 0000	 (NUL)*	 (DLE)*						
$A_6A_5A_4A_3$ 0001	 (SOH)*	 (DC1)*						
$A_6A_5A_4A_3$ 0010	 (STX)*	 (DC2)*						
$A_6A_5A_4A_3$ 0011	 (ETX)*	 (DC3)*						
$A_6A_5A_4A_3$ 0100	 (EOT)*	 (DC4)*						
$A_6A_5A_4A_3$ 0101	(ENQ)*	(NAK)*						
$A_6A_5A_4A_3$ 0110	(ACK)*	(SYN)*						
$A_6A_5A_4A_3$ 0111	(BEL)*	(ETB)*						

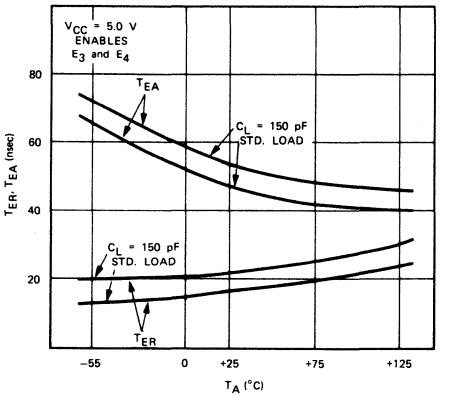
*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

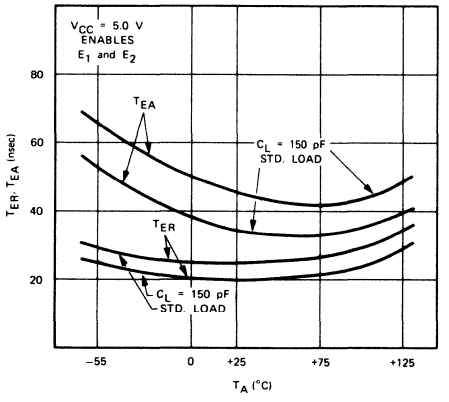
A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

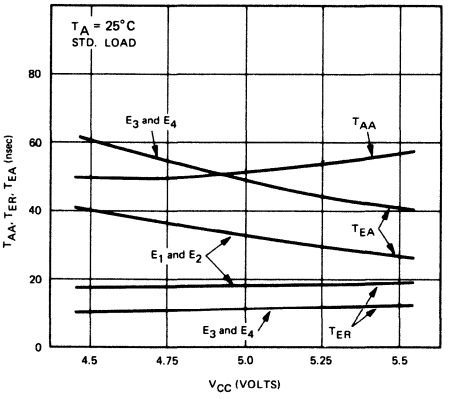
ASCII INPUT ADDRESS	$B_7B_6B_5$ $A_9A_8A_7$ 000	$A_9A_8A_7$ 001	$A_9A_8A_7$ 010	$A_9A_8A_7$ 011	$A_9A_8A_7$ 100	$A_9A_8A_7$ 101	$A_9A_8A_7$ 110	$A_9A_8A_7$ 111
$B_4B_3B_2B_1$ $A_6A_5A_4A_3$ 1000	 (BS)*	 (CAN)*						
$A_6A_5A_4A_3$ 1001	 (HT)*	 (EM)*						
$A_6A_5A_4A_3$ 1010	 (LF)*	 (SUB)*						
$A_6A_5A_4A_3$ 1011	 (VT)*	 (ESC)*						
$A_6A_5A_4A_3$ 1100	 (FF)*	 (FS)*						
$A_6A_5A_4A_3$ 1101	(CR)*	(GS)*						
$A_6A_5A_4A_3$ 1110	(SO)*	(RS)*						
$A_6A_5A_4A_3$ 1111	(SI)*	(US)*						(DEL)*

*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.









CHARACTER GENERATOR OPERATION

The intended application for the MM6062 is the generation of 128 USACII characters utilizing a readout system which generates the characters vertically a 7 bit line at a time. Each 35 bit character is composed of 7 distinct 5 bit lines. One of the 128 characters is selected by the 7 bit address applied to A_3 thru A_9. The particular 5 bit line within each character is determined by the 3 bit address applied to A_0, A_1 and A_2. The binary address 000 on A_0, A_1 and A_2 provides a blank line for character line spacing. The memory is enabled when either E_1 and E_2 are low (logic "0") or E_3 and E_4 are high (logic "1").

HIGH PERFORMANCE BIPOLAR 7×9 CHARACTER GENERATOR (ROW SCAN)

MM6071

USASCII 64 ALPHA-NUMERICS

Monolithic Memories
INCORPORATED

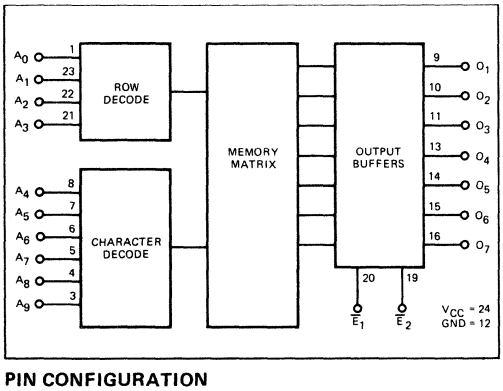
PRODUCT FEATURES

- 64 Alpha-Numerics in One Package
- Low Power Dissipation — 450mW
- Standard Packaging — 24 Pin Dip
- Single 5 Volt Supply
- 175 nsec Max. Access Time

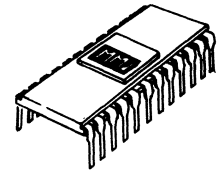
APPLICATIONS

- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting

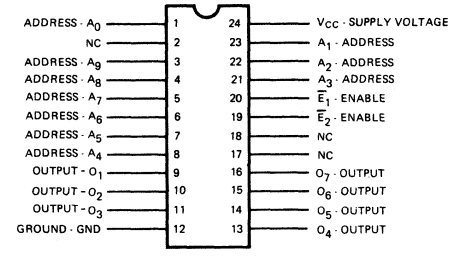
BLOCK DIAGRAM



PACKAGE CONFIGURATION

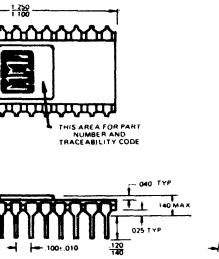


PIN CONFIGURATION



NOTE: A_0, A_1, A_2, A_3 are used for the character scan.

PACKAGE OUTLINE



Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

JUNE 1972

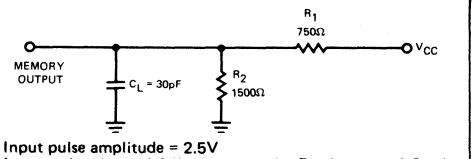
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Current	20mA
Output Current	100mA
Ambient Temperature	−65° to +125°C
Storage Temperature	−65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range, T_A	0° to 75°C
Supply Voltage	Max. 5.25V; Min. 4.75V

STANDARD TEST LOAD



Input pulse amplitude = 2.5V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4V
Output loading is 6mA and 30pF as given in std. load

*ELECTRICAL CHARACTERISTICS Memory outputs are open collector.

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
I_{FA}	Address Input Load Current	V_{CC} = 5.25V	V_A = 0.4V		−80	−250	μA
I_{FE}	Enable Input Load Current	V_{CC} = 5.25V	V_E = 0.4V		−80	−250	μA
I_{RA}	Address Input Leakage Current	V_{CC} = 5.25V	V_A = 2.4V			40	μA
I_{RE}	Enable Input Leakage Current	V_{CC} = 5.25V	V_E = 2.4V			40	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V	I_{OL} = 6mA		0.3	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0V			90	135	mA
V_{IL}	Low Level Input Voltage					0.8	V
V_{IH}	High Level Input Voltage			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = 5.25V	V_{CEX} = V_{CC} V			250	μA
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V	I_I = −5mA			−1.0	V
BV_I	Input Breakdown Voltage	V_{CC} = 5.25V	I_I = 1.0mA	5.5			V
C_I	Input Capacitance	V_{CC} = 5.0V	V_I = 2.0V		5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V	V_O = 2.0V		7.0		pF
		Output in High State					

*All limits apply for 5V ±5%, 0°C to 75°C

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

TEST	SYMBOL	CONDITIONS	TYP.	MAX.	UNITS
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	70	175	nsec
Enable Access Time	T_{EA}	Word Addressed is Storing a Low See Fig. 2	45	60	nsec
Enable Recovery Time	T_{ER}	Word Addressed is Storing a Low See Fig. 2	20	30	nsec

TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

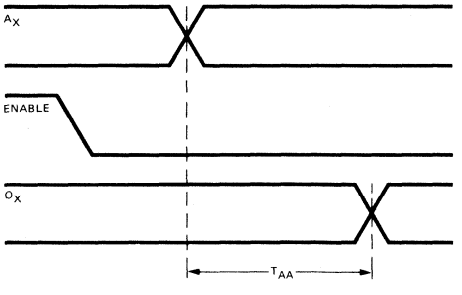
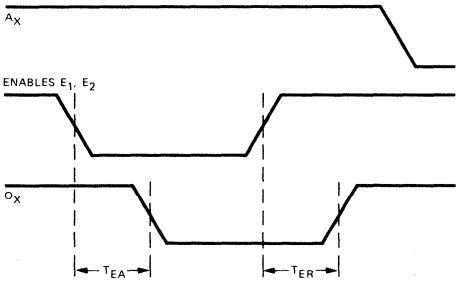
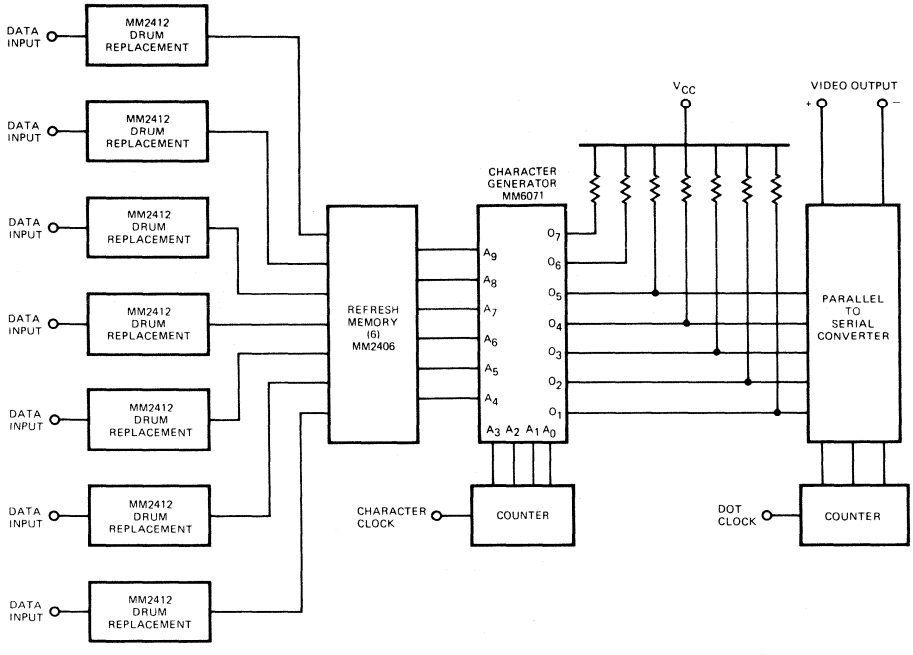


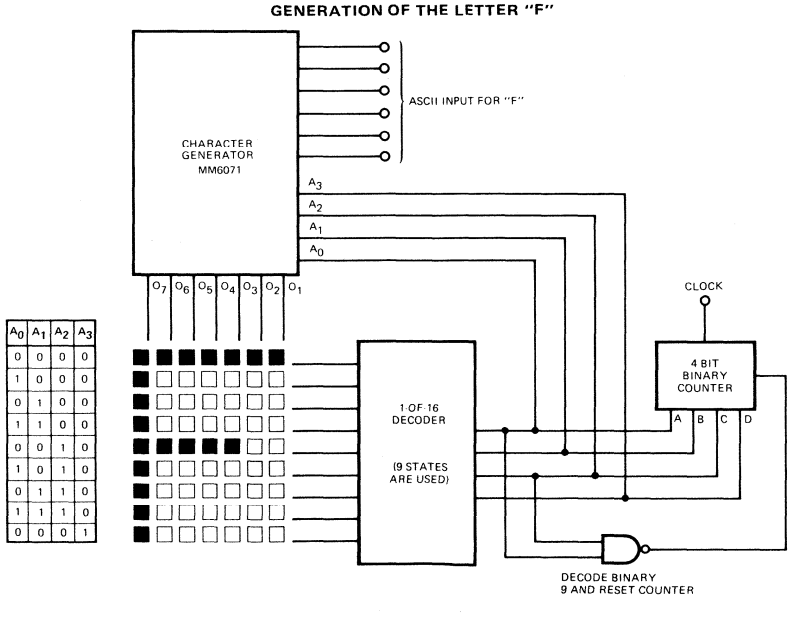
Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



CRT CHARACTER DISPLAY BLOCK DIAGRAM

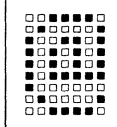
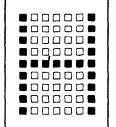
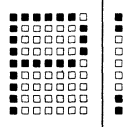
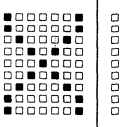
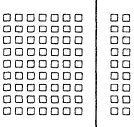
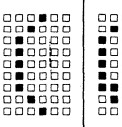
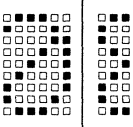
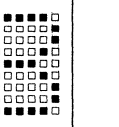
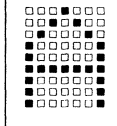
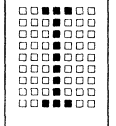
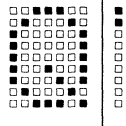
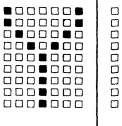
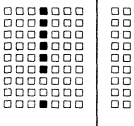
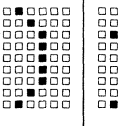
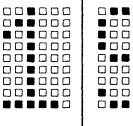
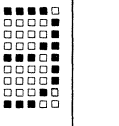
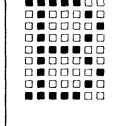
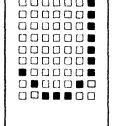
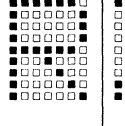
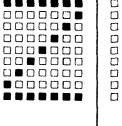
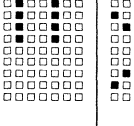
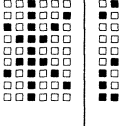
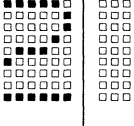
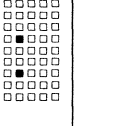
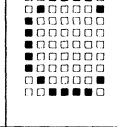
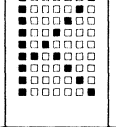
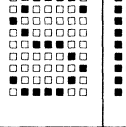
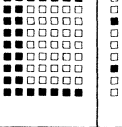
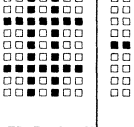
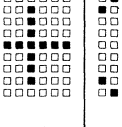
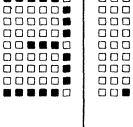
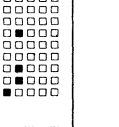
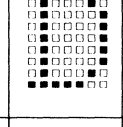
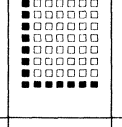
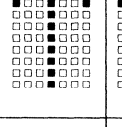
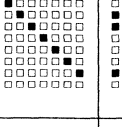
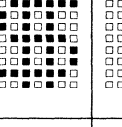
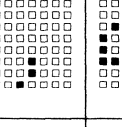
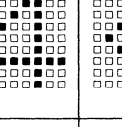
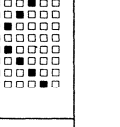


GENERATION OF THE LETTER "F"



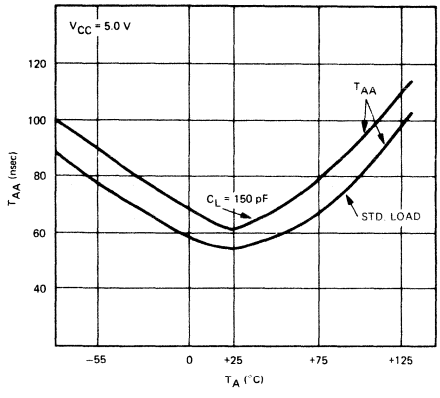
A_0	A_1	A_2	A_3
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1

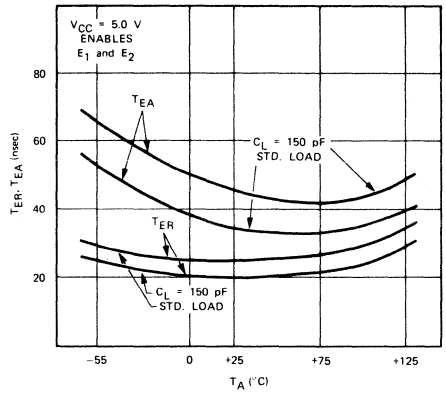
A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

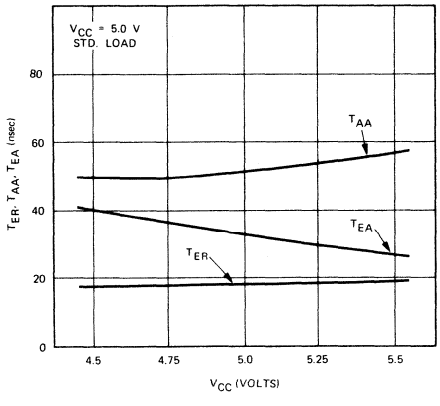
ASCII INPUT ADDRESS	B_5B_4 $A_9A_8A_7$ 000 $O_7O_6O_5O_4O_3O_2O_1$	B_5B_4 $A_9A_8A_7$ 001 $O_7O_6O_5O_4O_3O_2O_1$	B_5B_4 $A_9A_8A_7$ 010 $O_7O_6O_5O_4O_3O_2O_1$	B_5B_4 $A_9A_8A_7$ 011 $O_7O_6O_5O_4O_3O_2O_1$	B_5B_4 $A_9A_8A_7$ 100 $O_7O_6O_5O_4O_3O_2O_1$	B_5B_4 $A_9A_8A_7$ 101 $O_7O_6O_5O_4O_3O_2O_1$	B_5B_4 $A_9A_8A_7$ 110 $O_7O_6O_5O_4O_3O_2O_1$	B_5B_4 $A_9A_8A_7$ 111 $O_7O_6O_5O_4O_3O_2O_1$
$B_3B_2B_1$ $A_6A_5A_4$ 000								
$B_3B_2B_1$ $A_6A_5A_4$ 001								
$B_3B_2B_1$ $A_6A_5A_4$ 010								
$B_3B_2B_1$ $A_6A_5A_4$ 011								
$B_3B_2B_1$ $A_6A_5A_4$ 100								
$B_3B_2B_1$ $A_6A_5A_4$ 101								
$B_3B_2B_1$ $A_6A_5A_4$ 110								
$B_3B_2B_1$ $A_6A_5A_4$ 111								

* These representations were obtained from the USASI X 3.2 Code Practice Manual. Address $A_9 = B_7 = \overline{B_6}$.

CURVES







CHARACTER GENERATOR OPERATION

The intended application for the MM6071 is the generation of 64 USACII characters utilizing a readout system which generates the characters horizontally a 7 bit line at a time. Each 63 bit character is composed of 9 distinct 7 bit lines. One of the 64 characters is selected by the 6 bit address applied to A_4 thru A_9. The particular 7 bit line within each character is determined by the 4 bit address applied to A_0, A_1, A_2 and A_3. The binary addresses 9 thru 15 on A_0, A_1, A_2 and A_3 do not exist in the memory (since we want a 7 x 9 character) and will result in a low output if they are selected. Since the characters are produced by low outputs binary addresses 9 thru 15 should be avoided to eliminate confusion. This can be accomplished by "short counting" a 4 bit binary counter so that states 9 thru 15 don't exist. The memory is enabled when both E_1 and E_2 are low.

Monolithic
Memories
INCORPORATED

Printed in U.S.A.
2-4/5M/N

HIGH PERFORMANCE BIPOLAR 7×9 CHARACTER GENERATOR (ROW SCAN)

MM6072

USASCII 128 CHARACTERS

Monolithic Memories
INCORPORATED

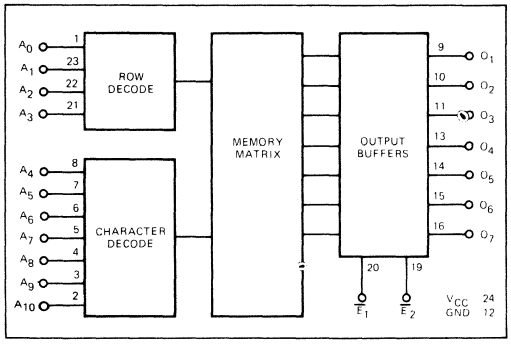
PRODUCT FEATURES

- 128 Characters in One Package
- Low Power Dissipation – 450mW
- Standard Packaging – 24 Pin Dip
- Single 5 Volt Supply
- 175 nsec Max. Access Time

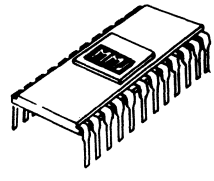
APPLICATIONS

- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting

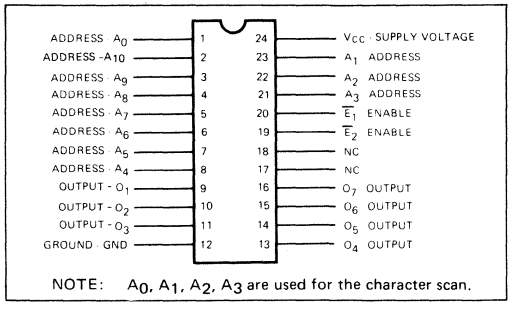
BLOCK DIAGRAM



PACKAGE CONFIGURATION

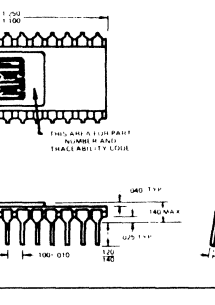


PIN CONFIGURATION



NOTE: A_0, A_1, A_2, A_3 are used for the character scan.

PACKAGE OUTLINE



Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

SEPTEMBER 1972

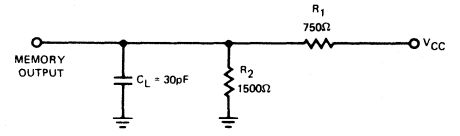
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Current	20mA
Output Current	100mA
Ambient Temperature	−65° to +125°C
Storage Temperature	−65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range, T_A	0° to 75°C
Supply Voltage	Max. 5.25V; Min. 4.75V

STANDARD TEST LOAD



Input pulse amplitude = 2.5V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4V
Output loading is 6mA and 30pF as given in std. load

*ELECTRICAL CHARACTERISTICS Memory outputs are open collector

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
I_{FA}	Address Input Load Current	V_{CC} = 5.25V	V_A = 0.4V		−80	−250	μA
I_{FE}	Enable Input Load Current	V_{CC} = 5.25V	V_E = 0.4V		−80	−250	μA
I_{RA}	Address Input Leakage Current	V_{CC} = 5.25V	V_A = 2.4V			40	μA
I_{RE}	Enable Input Leakage Current	V_{CC} = 5.25V	V_E = 2.4V			40	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V	I_{OL} = 6mA		0.3	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0V			90	135	mA
V_{IL}	Low Level Input Voltage					0.8	V
V_{IH}	High Level Input Voltage			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = 5.25V	V_{CEX} = V_{CC} V			250	μA
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V	I_I = −5mA			−1.0	V
BV_I	Input Breakdown Voltage	V_{CC} = 5.25V	I_I = 1.0mA	5.5			V
C_I	Input Capacitance	V_{CC} = 5.0V	V_I = 2.0V		5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V	V_O = 2.0V		7.0		pF
		Output in "O" State					

*All limits apply for 5V ± 5%, 0°C to 75°C

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

TEST	SYMBOL	CONDITIONS	TYP.	MAX.	UNITS
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	70	175	nsec
Enable Access Time	T_{EA}	Word Addressed is Storing a Low See Fig. 2	45	60	nsec
Enable Recovery Time	T_{ER}	Word Addressed is Storing a Low See Fig. 2	20	30	nsec

TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

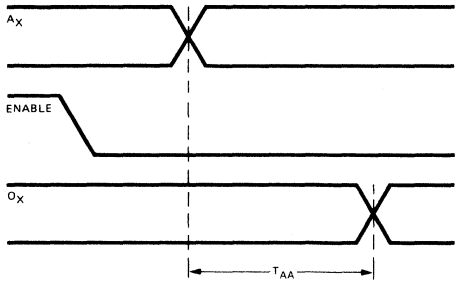
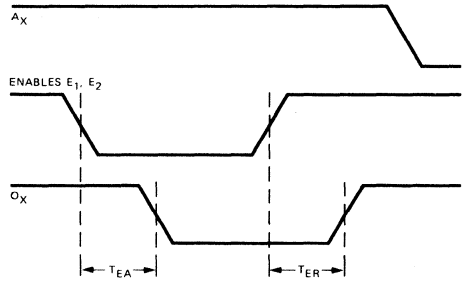
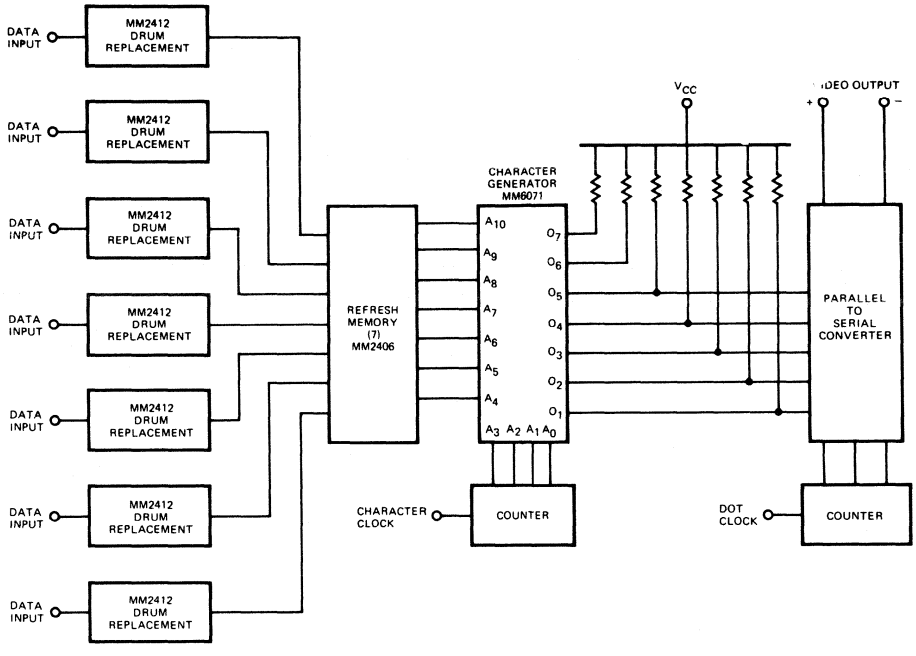


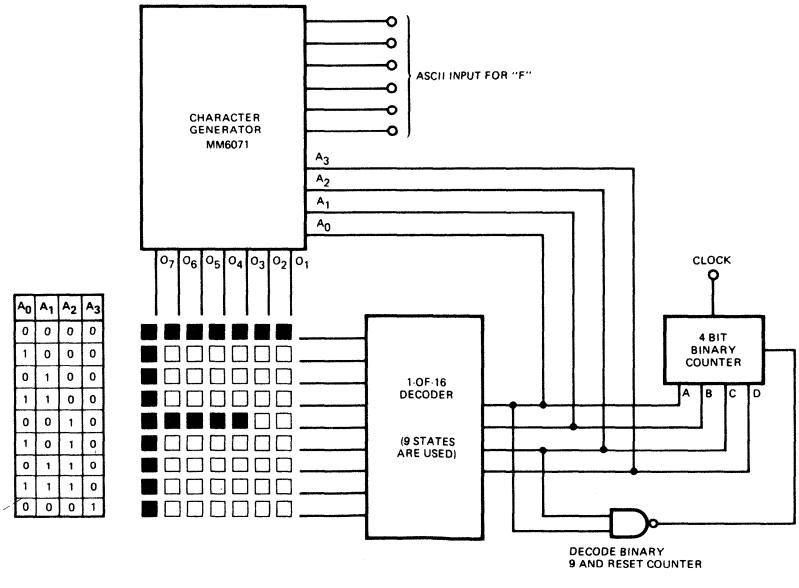
Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



CRT CHARACTER DISPLAY BLOCK DIAGRAM



GENERATION OF THE LETTER "F"



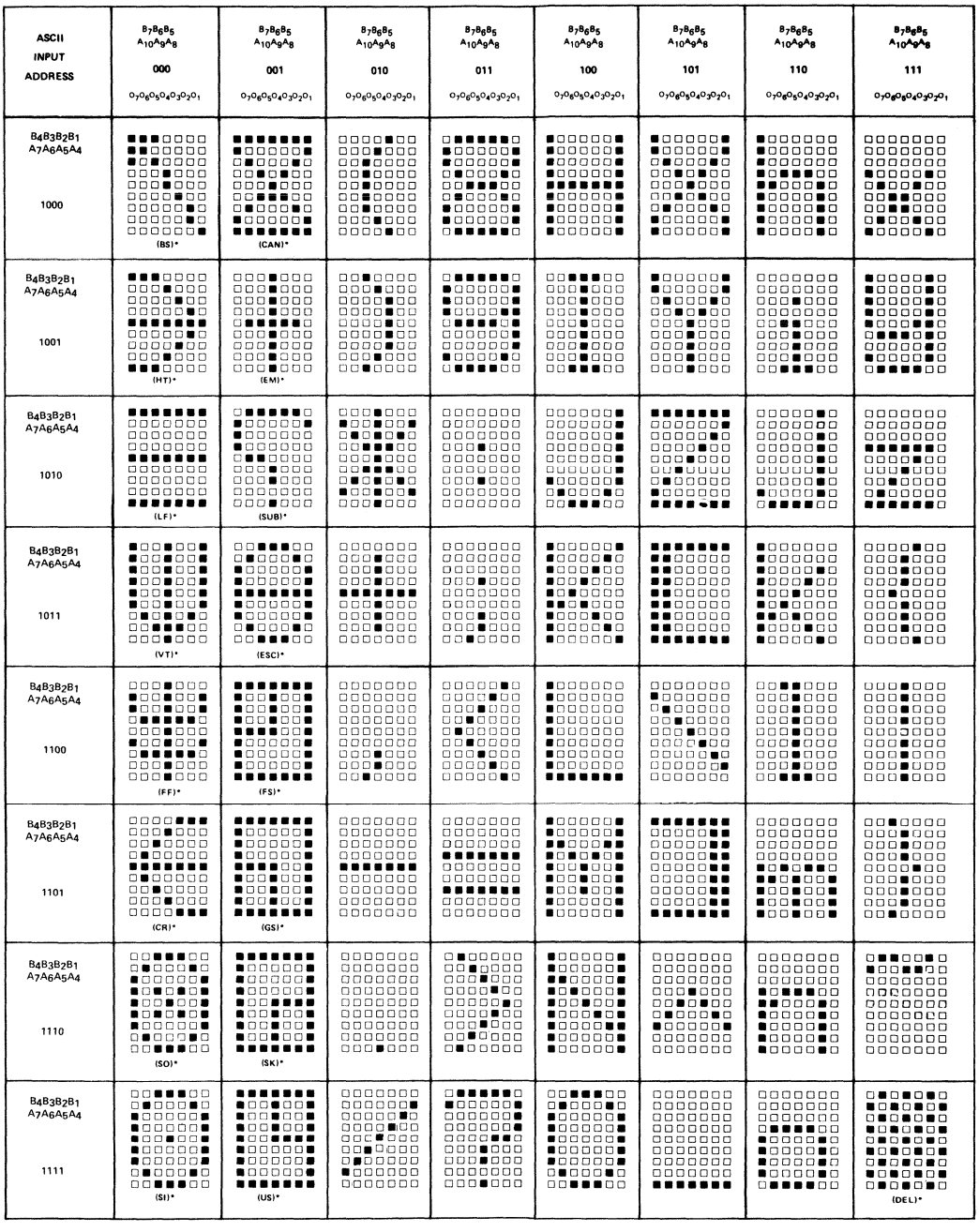
A_0	A_1	A_2	A_3
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1

A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

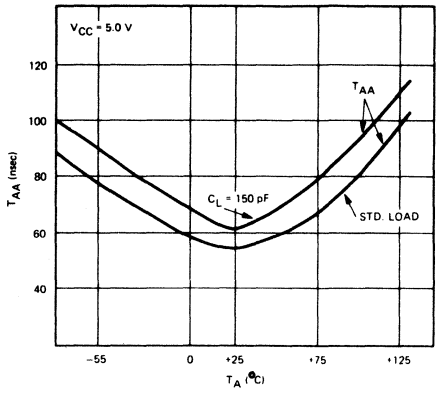
ASCII INPUT ADDRESS	$B_7B_6B_5$ $A_{10}A_9A_8$ 000 $O_7O_6O_5O_4O_3O_2O_1$	$B_7B_6B_5$ $A_{10}A_9A_8$ 001 $O_7O_6O_5O_4O_3O_2O_1$	$B_7B_6B_5$ $A_{10}A_9A_8$ 010 $O_7O_6O_5O_4O_3O_2O_1$	$B_7B_6B_5$ $A_{10}A_9A_8$ 011 $O_7O_6O_5O_4O_3O_2O_1$	$B_7B_6B_5$ $A_{10}A_9A_8$ 100 $O_7O_6O_5O_4O_3O_2O_1$	$B_7B_6B_5$ $A_{10}A_9A_8$ 101 $O_7O_6O_5O_4O_3O_2O_1$	$B_7B_6B_5$ $A_{10}A_9A_8$ 110 $O_7O_6O_5O_4O_3O_2O_1$	$B_7B_6B_5$ $A_{10}A_9A_8$ 111 $O_7O_6O_5O_4O_3O_2O_1$
$B_4B_3B_2B_1$ $A_7A_6A_5A_4$ 0000	(NUL)*	(DLE)*						
$B_4B_3B_2B_1$ $A_7A_6A_5A_4$ 0001	(SOH)*	(DC1)*						
$B_4B_3B_2B_1$ $A_7A_6A_5A_4$ 0010		(DC2)*						
$B_4B_3B_2B_1$ $A_7A_6A_5A_4$ 0011	(ETX)*	(DC3)*						
$B_4B_3B_2B_1$ $A_7A_6A_5A_4$ 0100	(EOT)*	(DC4)*						
$B_4B_3B_2B_1$ $A_7A_6A_5A_4$ 0101	(ENQ)*	(NAK)*						
$B_4B_3B_2B_1$ $A_7A_6A_5A_4$ 0110	(ACK)*	(SYN)*						
$B_4B_3B_2B_1$ $A_7A_6A_5A_4$ 0111	(BEL)*	(ETB)*						

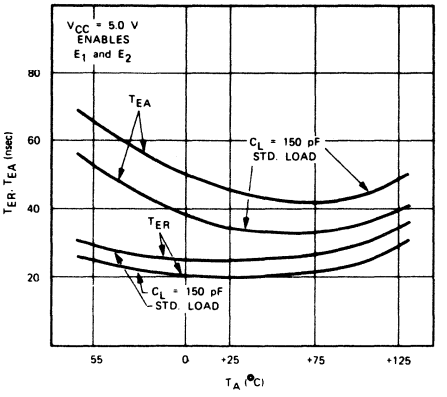
* The letters in parenthesis identify the control code corresponding to the appropriate 63 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

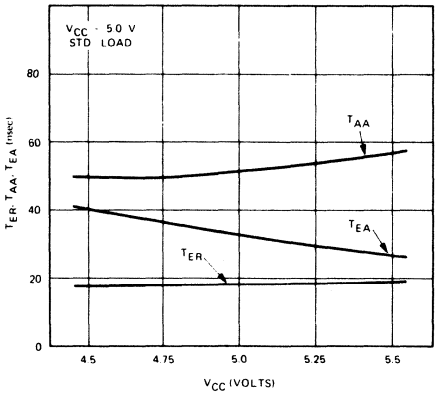
A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT



* The letters in parenthesis identify the control code corresponding to the appropriate 63 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.







CHARACTER GENERATOR OPERATION

The intended application for the MM6072 is the generation of 128 USACII characters utilizing a readout system which generates the characters horizontally a 7 bit line at a time. Each 63 bit character is composed of 9 distinct 7 bit lines. One of the 128 characters is selected by the 7 bit address applied to A_4 thru A_{10}. The particular 7 bit line within each character is determined by the 4 bit address applied to A_0, A_1, A_2 and A_3. The binary addresses 9 thru 15 on A_0, A_1, A_2 and A_3 do not exist in the memory (since we want a 7 x 9 character) and will result in a low output if they are selected. Since the characters are produced by low outputs binary addresses 9 thru 15 should be avoided to eliminate confusion. This can be accomplished by "short counting" a 4 bit binary counter so that states 9 thru 15 don't exist. The MM6072 is an 1152 word ROM (128 characters at 9 rows each) and words 1152 thru 2047 do not exist and should be avoided. The memory is enabled when both E_1 and E_2 are low.

HIGH PERFORMANCE BIPOLAR 7×9 CHARACTER GENERATOR (COLUMN SCAN)

MM6073

USASCII 128 CHARACTERS

Monolithic Memories
INCORPORATED

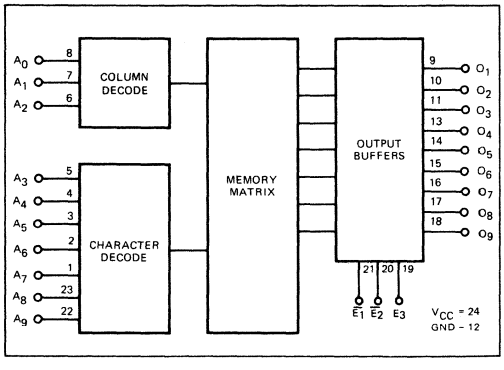
PRODUCT FEATURES:

- 128 Characters in One Package
- Low Power Dissipation – 450mW
- Standard Packaging – 24 Pin Dip
- Single 5 Volt Supply
- 175 nsec Max. Access Time

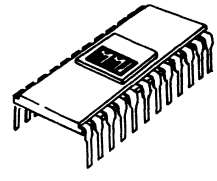
APPLICATIONS:

- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting

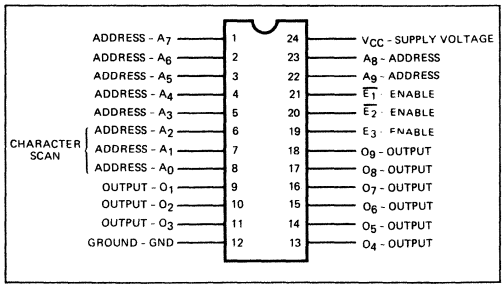
BLOCK DIAGRAM



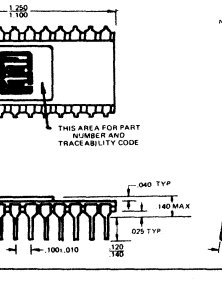
PACKAGE CONFIGURATION



PIN CONFIGURATION



PACKAGE OUTLINE



Monolithic Memories
INCORPORATED

1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

SEPTEMBER 1972

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Current	20mA
Output Current	100mA
Ambient Temperature	−65° to +125°C
Storage Temperature	−65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range, T_A	0° to 75°C
Supply Voltage	Max. 5.25V; Min. 4.75V

ELECTRICAL CHARACTERISTICS - Memory outputs are open collector

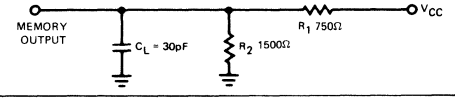
PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
I_{FA}	Address Input Load Current	V_{CC} = 5.25V	V_A = 0.4V		−80	−250	μA
I_{FE}	Enable Input Load Current	V_{CC} = 5.25V	V_E = 0.4V		−80	−250	μA
I_{RA}	Address Input Leakage Current	V_{CC} = 5.25V	V_A = 2.4V			40	μA
I_{RE}	Enable Input Leakage Current	V_{CC} = 5.25V	V_E = 2.4V			40	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V	I_{OL} = 6mA		0.3	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0V			90	135	mA
V_{IL}	Low Level Input Voltage					0.8	V
V_{IH}	High Level Input Voltage			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = 5.25V	V_{CEX} = V_{CC} V			250	μA
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V	I_I = −5mA			−1.0	V
BV_I	Input Breakdown Voltage	V_{CC} = 5.25V	I_I = 1.0mA	5.5			V
C_I	Input Capacitance	V_{CC} = 5.0V	V_I = 2.0V		5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V Output in HIGH State	V_O = 2.0V		7.0		pF

*All limits apply for 5V ± 5%, 0°C to 75°C

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

TEST	SYMBOL	CONDITIONS	TYP.	MAX.	UNITS
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	60	175	nsec
Enable Access Time	T_{EA}	Word Addressed is Storing a Low See Fig. 2	35	60	nsec
Enable Recovery Time	T_{ER}	Word Addressed is Storing a Low See Fig. 2	20	30	nsec

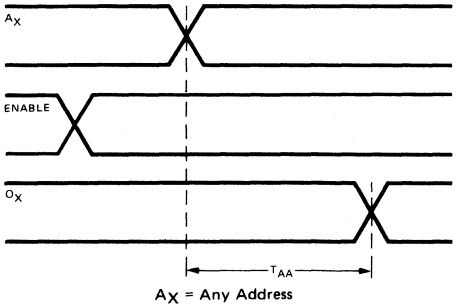
STANDARD TEST LOAD



Input pulse amplitude = 2.5V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4V
Output loading is 6mA and 30pF as given in std. load

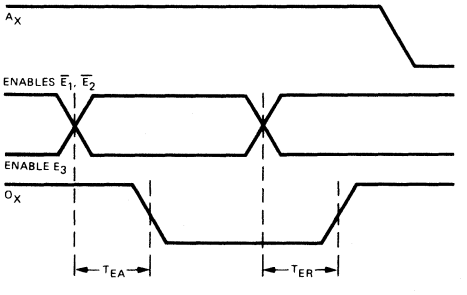
TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

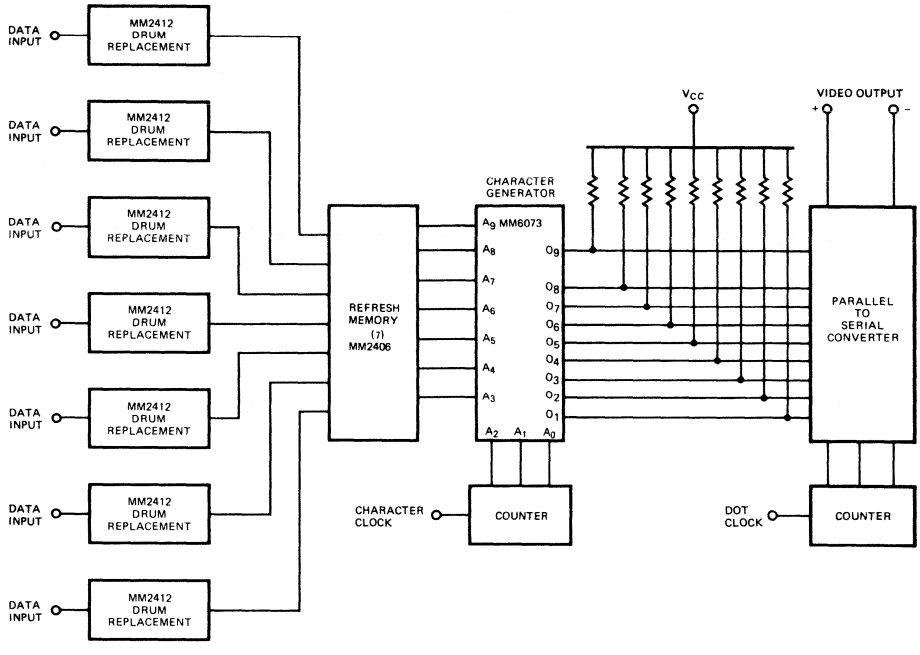


A_X = Any Address
O_X = Any Output

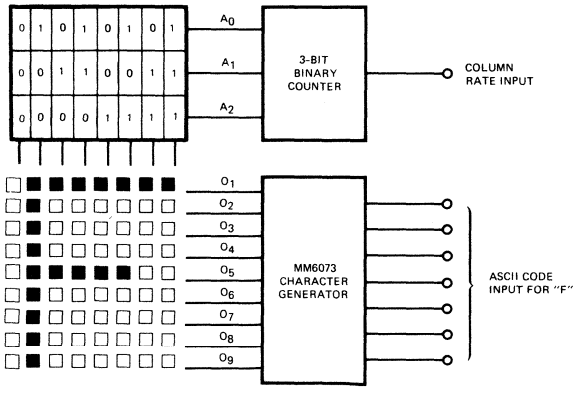
Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



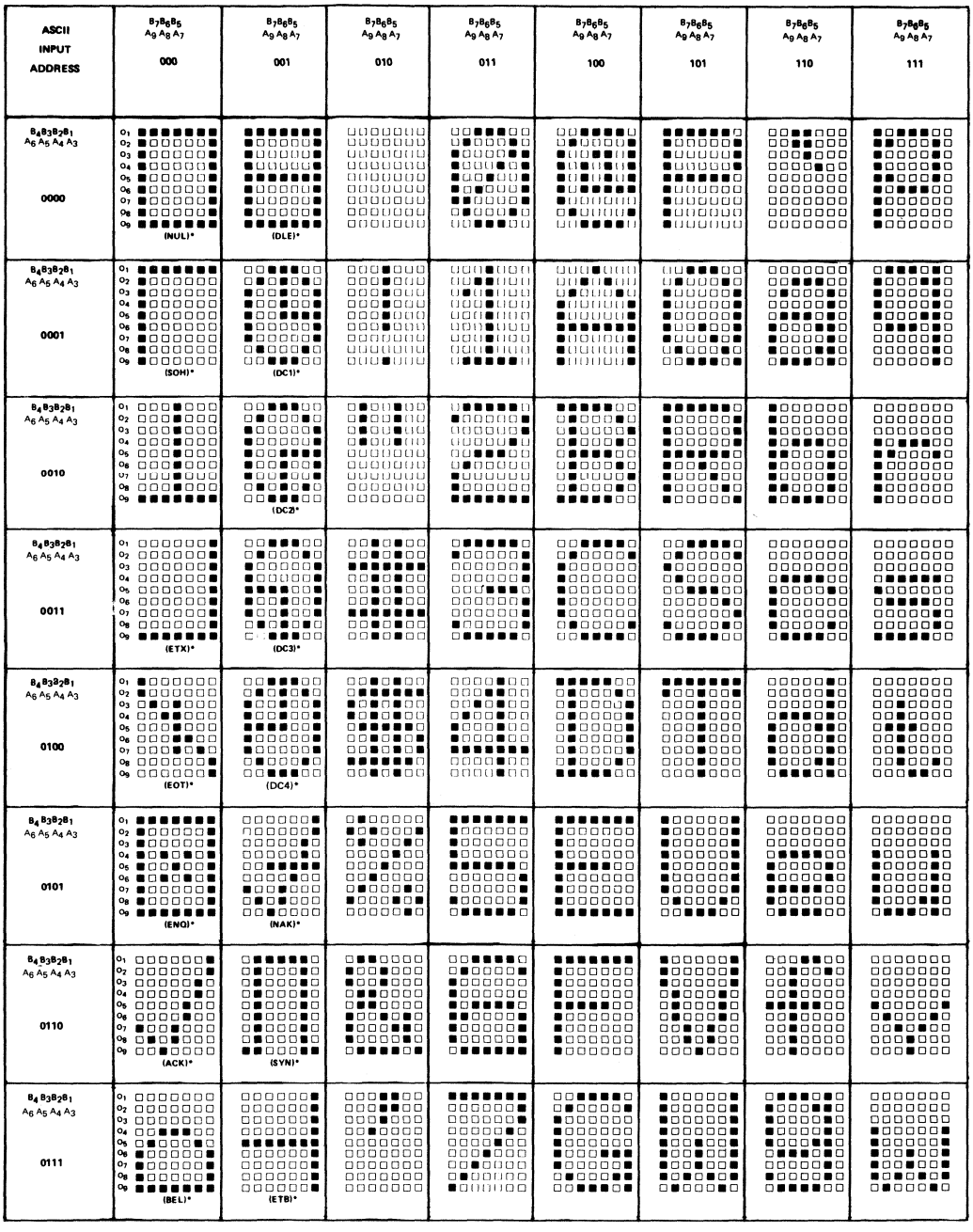
CRT CHARACTER DISPLAY BLOCK DIAGRAM



GENERATION OF THE LETTER "F"

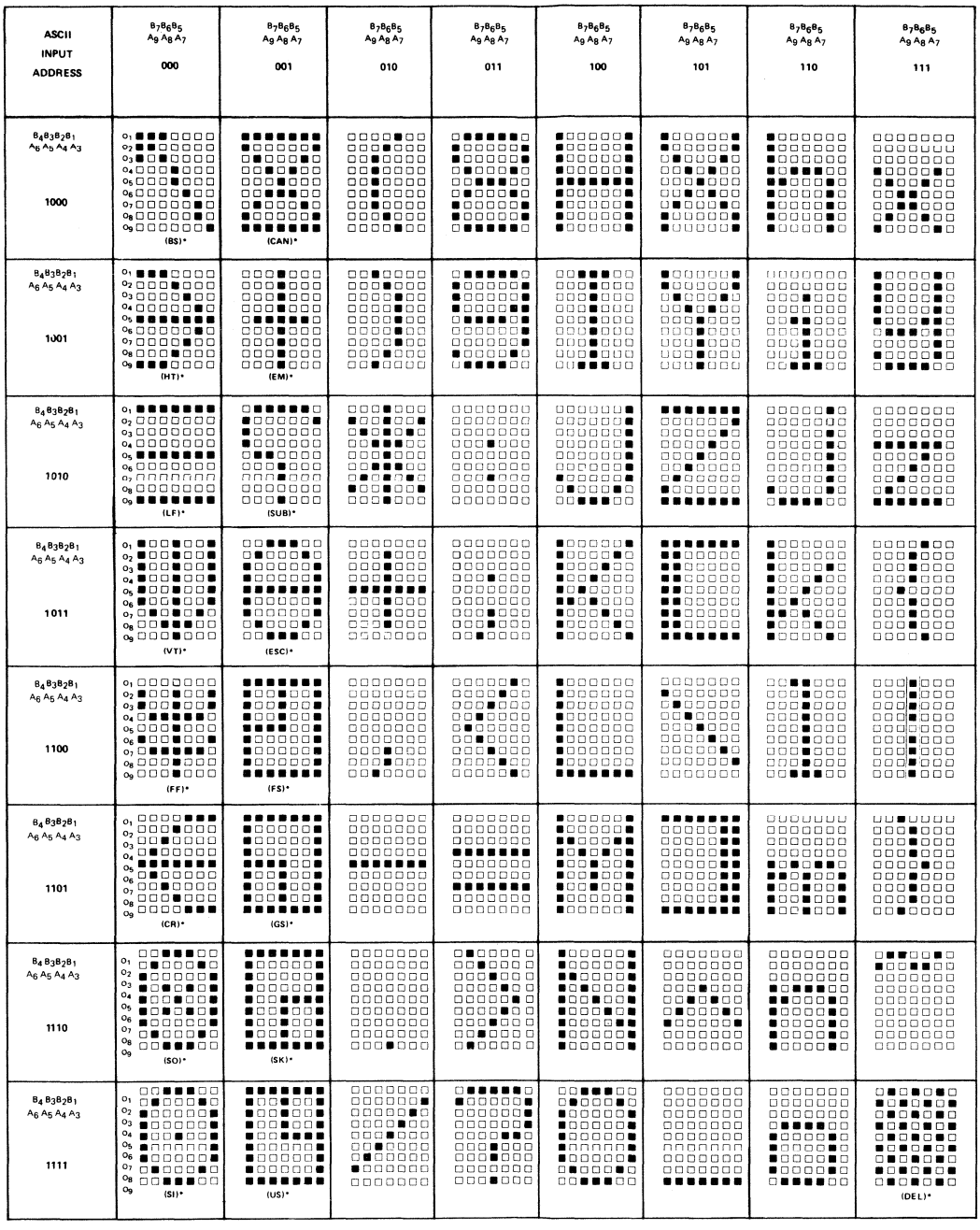


A "filled in" dot represents a low memory output.

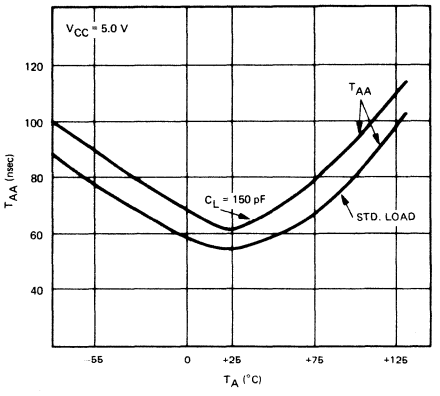


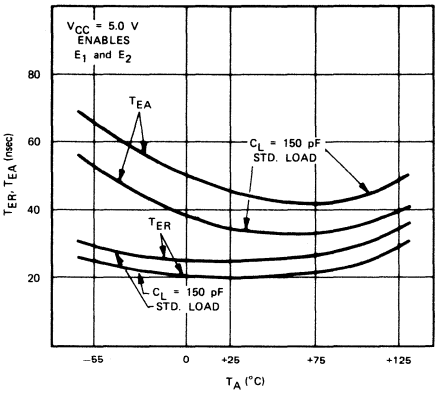
* The letters in parenthesis identify the control code corresponding to the appropriate 63 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

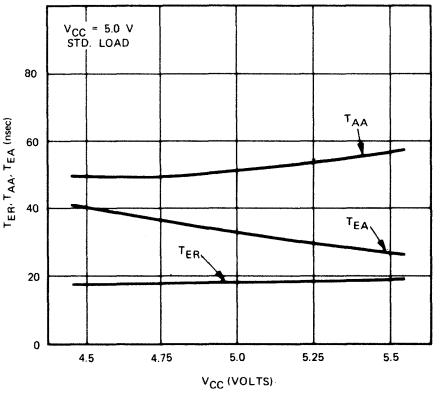
A "filled in" dot represents a low memory output.



* The letters in parenthesis identify the control code corresponding to the appropriate 63 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.







CHARACTER GENERATOR OPERATION

The intended application for the MM6073 is the generation of 128 USACII characters utilizing a readout system which generates the characters vertically a 9 bit column at a time. Each 63 bit character is composed of 7 distinct 9 bit lines. One of the 128 characters is selected by the 7 bit address applied to A_3 thru A_9. The particular 9 bit column within each character is determined by the 3 bit address applied to A_0, A_1 and A_2. The binary address 000 on A_0, A_1 and A_2 provides a blank line for character line spacing. The memory is enabled when both E_1 and E_2 are low and E_3 is high.

SINE (0° TO 90°) LOOK UP TABLE USING A (1024 X 10) BIPOLAR ROM (5255/6255)

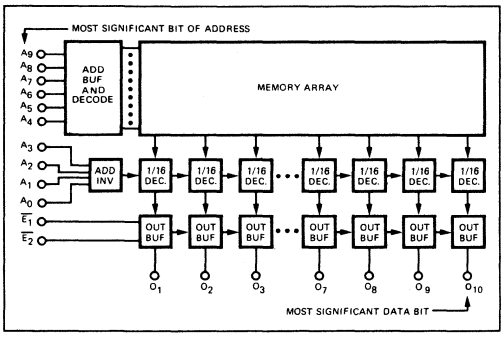
5086/6086

Monolithic Memories
INCORPORATED

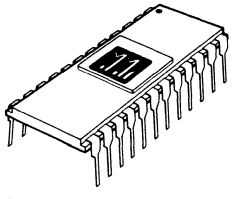
PRODUCT FEATURES

- Input angle increments of 90°/1024 = .0879°
- 10 bit binary outputs
- Low power dissipation. Typically 500 mw
- Fast access time 150 ns max.
- DTL and TTL compatible
- Two enable inputs
- Open collectors outputs
- Advanced Schottky processing

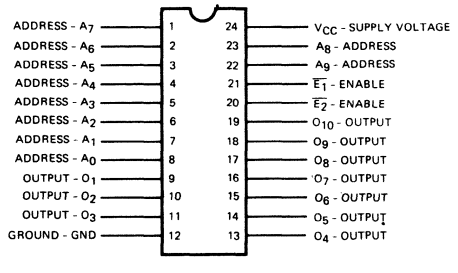
BLOCK DIAGRAM: 1024 WORDS X 10 BITS MEMORY



PACKAGE CONFIGURATION



PIN CONFIGURATION

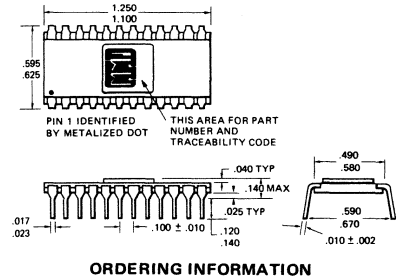


ENABLE = $\overline{E_1}$ LOW AND $\overline{E_2}$ LOW

PACKAGE OUTLINE

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 48°C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt.



ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6086D

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

NOVEMBER 1973

ELECTRICAL PARAMETERS – SWITCHING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	–0.5 to 7V	Operating Free-Air	5086	–55 to +125°C
Input Current	20 mA	Temperature Range T_A	6086	0 to 75°C
Output Current	100 mA	Supply Voltage	5086	4.5 to 5.5V
Ambient Temperature	–65 to +125°C	(Min to Max)	6086	4.75 to 5.25V
Storage Temperature	–65 to +150°C			

*ELECTRICAL CHARACTERISTICS – Memory outputs are open collector

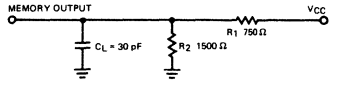
*All limits apply for 5V ±5%, 0°C to 75°C for the 6086. All limits apply for 5V ±10%, –55°C to 125°C for the 5086.

PARAMETER		CONDITIONS	5086			6086			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All inputs	V_{CC} = Max, V_F = 0.45 V			–250			–250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 6 mA		0.35	0.50				V
		V_{CC} = Min, I_{OL} = 6 mA					0.35	0.50	V
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs at 2.4 V All Outputs Open		100	150		100	150	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current High Stored or Disabled	V_{CC} = Max, V_{CEX} = 2.40 V			250			250	μA
		V_{CC} = Max = V_{CEX}			1			1	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = –5 mA		1.0	–1.5		–1.0	–1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

TEST	SYMBOL	CONDITIONS	5086		6086		UNITS
			TYP.	MAX	TYP.	MAX	
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	100	150	100	150	ns
Enable Recovery Time	T_{ER}	Word Addressed is Storing a low. See Fig. 2		60		60	ns
Enable Access Time	T_{EA}	Word Addressed is Storing a low. See Fig. 2		60		60	ns

STANDARD TEST LOAD



Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5 ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 6 mA and 30 pF as given in std. load

TEST WAVEFORMS

Fig. 1
ADDRESS ACCESS TIME

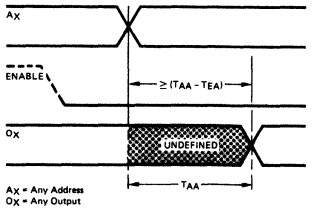
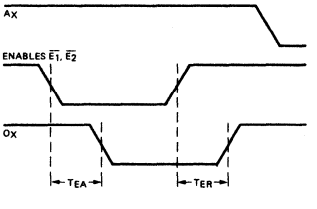


Fig. 2
ENABLE ACCESS TIME AND RECOVERY TIME



GENERAL DESCRIPTION

The 5255/6255, 1024 words by 10 bits Read Only Memory has been customized to make a sine θ look up table (5086/6086) for $0^\circ \leq \theta < 90^\circ$. The address inputs are used to divide the first 90° quadrant into angles increments of 90°/1024 words or .0879°/word. The memory outputs should be interpreted as binary weighted fractions where output 1 has a weight of 1/2 or .500, output 2 has a weight of 1/4 or .250, and so on until output 10 which has a weight of 1/1024 or .000976. The 10 bit output code has not been rounded off so that output error will always be positive and less than 1/1024 or .0009765. Round off error, in approximating the ROM input word, must be added or subtracted to the output error.

EXAMPLE 1:

Find the sine 45°

Let X = the ROM word where sine 45° is stored

$$\frac{X}{1024 \text{ words}} = \frac{45^\circ}{90^\circ}$$

X = word 512

Word 511 has the following stored data and interpretation:

Output #	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_8	0_9	0_{10}	
Stored Data	H	L	H	H	L	H	L	H	L	L	(H = TTL HIGH)
Binary Weight	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512	1/1024	

Adding the fractions wherever an "H" appears given.

$$\frac{1}{2} + \frac{1}{8} + \frac{1}{16} + \frac{1}{64} + \frac{1}{256} = .50000 + .12500 + .06250 + .01562 + .00391 = .70507$$

Handbook Value = .70711

Our Error = .70711 −.70703 = .00008

EXAMPLE 2:

Find the sine 210°

This value is in quadrant three, therefore, $\theta' = 210^\circ - 180^\circ$ or 30°

Let X = the ROM word where sine 30° is stored $\frac{X}{1024 \text{ words}} = \frac{30^\circ}{90^\circ}$

X = word 341.33 (round off to word 341)

Word 341's stored data = 0_1 0_2 0_3 0_4 0_5 0_6 0_7 0_8 0_9 0_{10}

Binary Weight = 1/2 1/4 1/8 1/16 1/32 1/64 1/128 1/256 1/512 1/1024

= .49902

The sine 210°, therefore, = −.49902 with the sign generated by external logic. Note that the address 341 which we rounded off to is actually the sine 29.97°.

MEMORY OPERATION

The memory addressing uses inputs A_0 through A_9 which selects 1 of 1024 words for read out of ten bits on the outputs (0_1–0_{10}). Additional blocks of ten bits by 1024 words may be added by driving additional packages with the respective address and enable lines. The memory is enabled when both $\overline{E_1}$ and $\overline{E_2}$ are LOW. When the memory is not enabled, its open collector output transistors are held off permitting wire ORing.

4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

MM6084/74284
MM6085/74285
MM5084/54284
MM5085/54285

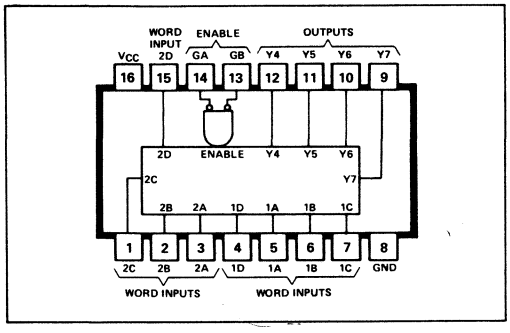
Monolithic Memories
INCORPORATED

The 54284 and 54285 are the military (5V±10%, −55°C to 125°C) versions of the 74284 and 74285 which are 5V±5%, 0°C to 75°C. Add a suffix N for a plastic package. The 6084, 6085, 5084, and 5085 are Monolithic Memories internal part number.

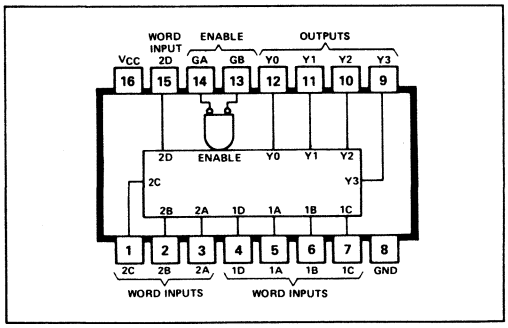
PRODUCT FEATURES

- **A 4x4 multiplier in two 16 pin packages**
- **Fast multiplication of two binary numbers**
  8 bit product in 40 ns typical
- **Expandable for N-BIT-by-M-BIT applications**
  16 bit product in 70 ns typical
  32 bit product in 103 ns typical

54284/74284

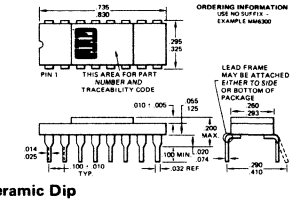


54285/74285

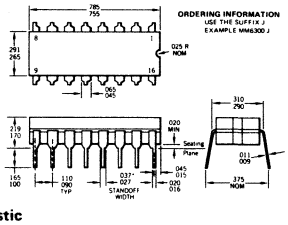


PACKAGE OUTLINE

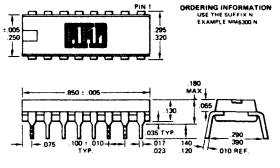
16 Pin Ceramic (Metal Cap)



16 Pin Ceramic Dip



16 Pin Plastic



Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

MARCH 1974

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7 V
Input Current	20 mA
Output Current	100 mA
Ambient Temperature	-65 to +125°C
Storage Temperature	-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range T_A	54284/54285	-55 to +125°C
	74284/74285	0 to 75°C
Supply Voltage (Min to Max)	54284/54285	4.5 to 5.5 V
	74284/74285	4.75 to 5.25 V

ELECTRICAL CHARACTERISTICS — SEE NOTE*

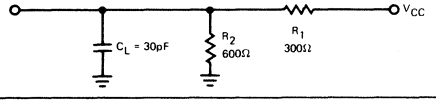
PARAMETER		CONDITIONS	54284/54285			74284/74285			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_F	Input Load Current All Inputs	V_{CC} = Max, V_F = 0.45 V		−1.0	−1.6		−1.0	−1.6	mA
I_R	Input Leakage Current All Inputs	V_{CC} = Max, V_1 = 2.4 V			40			40	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 10 mA		0.25	0.45				
		V_{CC} = Min, I_{OL} = 16 mA					0.3	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, All Inputs Open		70	125		70	125	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.8			0.85	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 5.5 V			100			100	μA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA			−1.5			−1.5	V
BV_I	Breakdown Voltage All Inputs	V_{CC} = Max, I_I = 1.0 mA	5.0			5.0			V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V		5.0			5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V Output in High State		7.0			7.0		pF

All limits apply for V_{CC} = 5.0V±5%, T_A = 0°C to 75°C for the 74284/74285 and V_{CC} = 5V±10%, T_A = -55°C to 125°C for the 54284/54285

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0 V, Std. Load)

TEST	SYMBOL	CONDITIONS	TYP.	MAX.	UNITS
Propagation Delay From Word Inputs	T_{DW}	Any Word Input to Any Output See Fig. 1	35	60	ns
Enable Delay Time	T_{ED}	Output is a Low See Fig. 2	21	30	ns
Enable Recovery Time	T_{ER}	Output is a Low See Fig 2.	21	30	ns

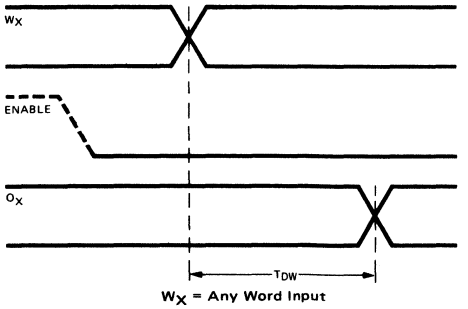
STANDARD TEST LOAD



Input pulse amplitude = 2.5 V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4 V
Output loading is 15 mA and 30 pF as given in std. load

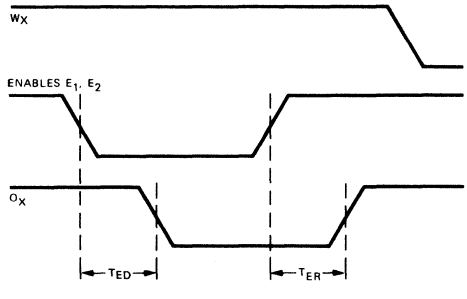
TEST WAVEFORMS

Fig. 1
PROPAGATION DELAY



W_X = Any Word Input
O_X = Any Output

Fig. 2
ENABLE DELAY TIME AND RECOVERY TIME



DESCRIPTION

The 54284/74284 and the 54285/74285 are designed to be used together to form a positive logic parallel multiplication of two 4 bit binary words as shown in Figure A. The eight bit binary product is typically generated in 40 nanoseconds. Both enable GA and GB must be low to activate the part.

This basic four by four multiplier can be used as a building block for implementing larger multipliers. For example, Figure B shows an 8x8 multiplier built from 4x4 multipliers and TTL adders to sum the partial products. The 16 bit product of the two eight bit words will typically be generated in 65 nanoseconds. The scheme is expandable for NXM bit multipliers.

MULTIPLIER

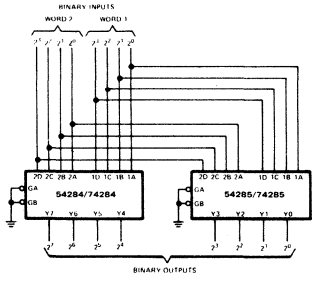


Fig. A - 4 X 4 MULTIPLIER

Fig. B - 8 X 8 MULTIPLIER

†Other terminals of the three SN54S181/SN74S181 ALU's are connected as follows: S3 = H, S2 = L, S1 = L, S0 = H, M = L. Output A = B is not used for this application.

HIGH PERFORMANCE BIPOLAR 7×9 CHARACTER GENERATOR (COLUMN SCAN)

MM6074

USASCII 64 ALPHA-NUMERICS

Monolithic Memories
INCORPORATED

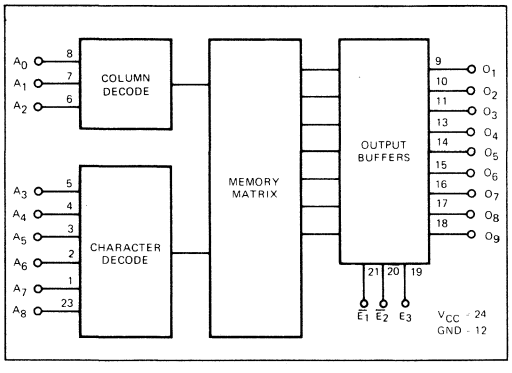
PRODUCT FEATURES:

- 64 Alpha Numerics in One Package
- Low Power Dissipation – 450mW
- Standard Packaging – 24 Pin Dip
- Single 5 Volt Supply
- 175 nsec Max. Access Time

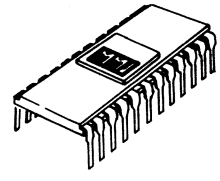
APPLICATIONS:

- A Single Package High Speed Bipolar Replacement For Slow Multiple Package MOS Character Generators
- CRT Displays
- Printing Calculators
- LED Arrays
- Typesetting

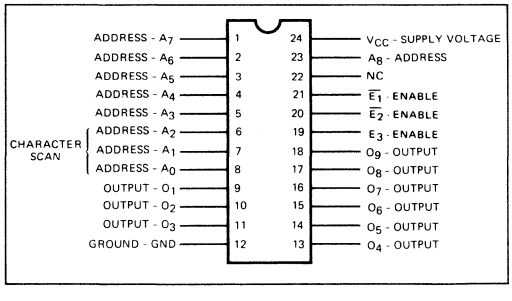
BLOCK DIAGRAM



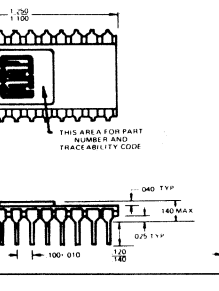
PACKAGE CONFIGURATION



PIN CONFIGURATION



PACKAGE OUTLINE



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TWX 910–339-9229

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Current	20mA
Output Current	100mA
Ambient Temperature	−65° to +125°C
Storage Temperature	−65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Operating Free-Air Temperature Range, T_A	0° to 75°C
Supply Voltage	Max. 5.25V; Min. 4.75V

*ELECTRICAL CHARACTERISTICS - Memory outputs are open collector

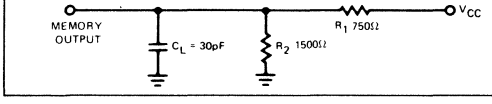
PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
I_{FA}	Address Input Load Current	V_{CC} = 5.25V	V_A = 0.4V		−80	−250	μA
I_{FE}	Enable Input Load Current	V_{CC} = 5.25V	V_E = 0.4V		−80	−250	μA
I_{RA}	Address Input Leakage Current	V_{CC} = 5.25V	V_A = 2.4V			40	μA
I_{RE}	Enable Input Leakage Current	V_{CC} = 5.25V	V_E = 2.4V			40	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V	I_{OL} = 6mA		0.3	0.45	V
I_{CC}	Power Supply Current	V_{CC} = 5.0V			90	135	mA
V_{IL}	Low Level Input Voltage					0.8	V
V_{IH}	High Level Input Voltage			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = 5.25V	V_{CEX} = V_{CC} V			250	μA
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V	I_I = −5mA			−1.0	V
BV_I	Input Breakdown Voltage	V_{CC} = 5.25V	I_I = 1.0mA	5.5			V
C_I	Input Capacitance	V_{CC} = 5.0V	V_I = 2.0V		5.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V	V_O = 2.0V		7.0		pF
		Output in HIGH State					

*All limits apply for 5V ± 5%, 0°C to 75°C

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = 5.0V, Std. Load)

TEST	SYMBOL	CONDITIONS	TYP.	MAX.	UNITS
Address Access Time	T_{AA}	Any Address Reading "0" or "1" See Fig. 1	60	175	nsec
Enable Access Time	T_{EA}	Word Addressed is Storing a Low See Fig. 2	35	60	nsec
Enable Recovery Time	T_{ER}	Word Addressed is Storing a Low See Fig. 2	20	30	nsec

STANDARD TEST LOAD

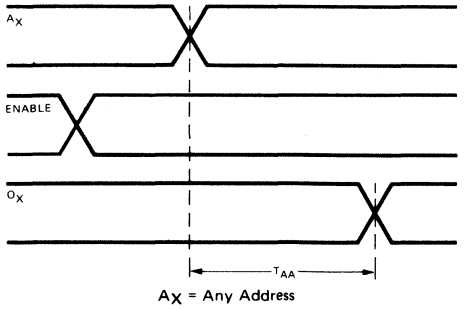


Input pulse amplitude = 2.5V
Input pulse rise and fall times must be 5ns between 1.0 volt and 2.0 volts
Speed measurements are made at 1.4V
Output loading is 6mA and 30pF as given in std. load

TEST WAVEFORMS

Fig. 1

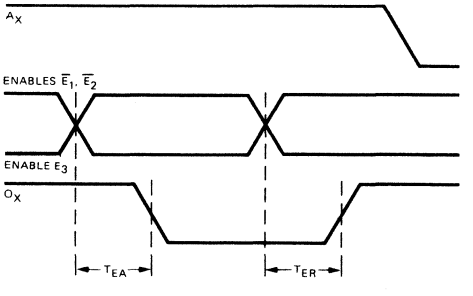
ADDRESS ACCESS TIME



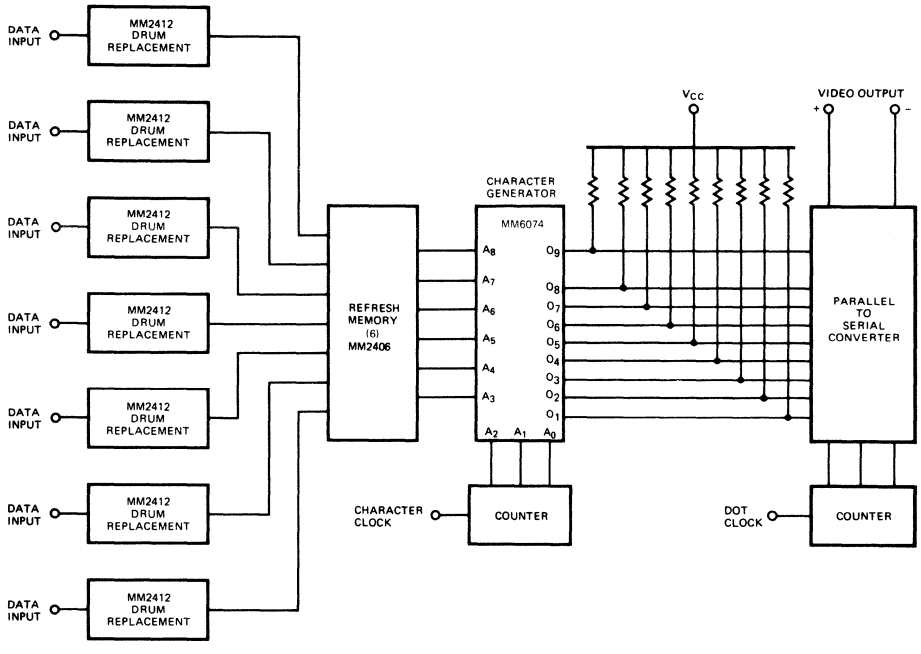
A_X = Any Address
O_X = Any Output

Fig. 2

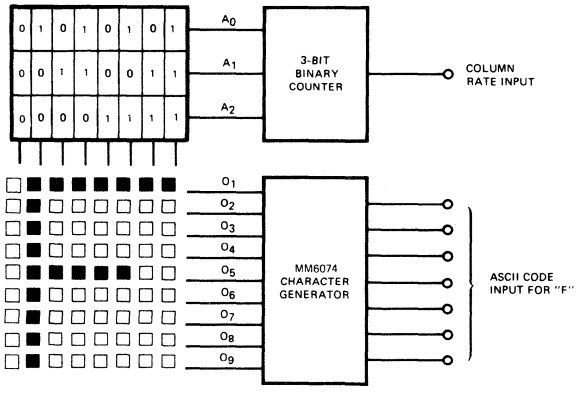
ENABLE ACCESS TIME AND RECOVERY TIME



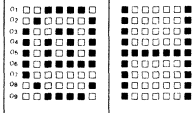
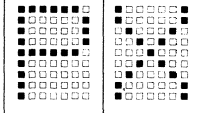
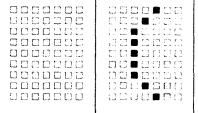
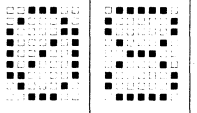
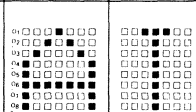
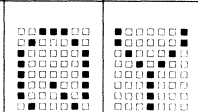
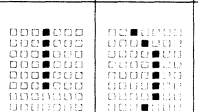
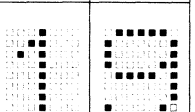
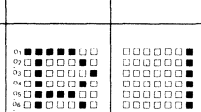
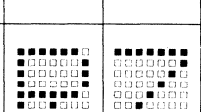
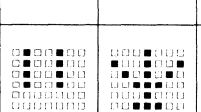
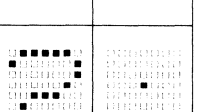
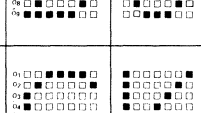
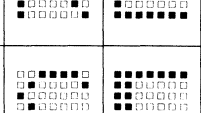
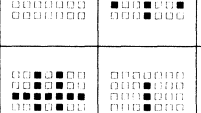
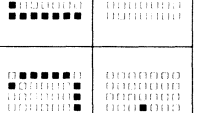
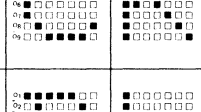
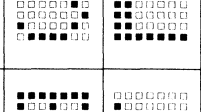
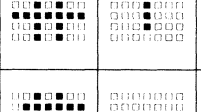
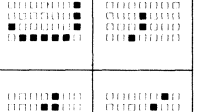
CRT CHARACTER DISPLAY BLOCK DIAGRAM



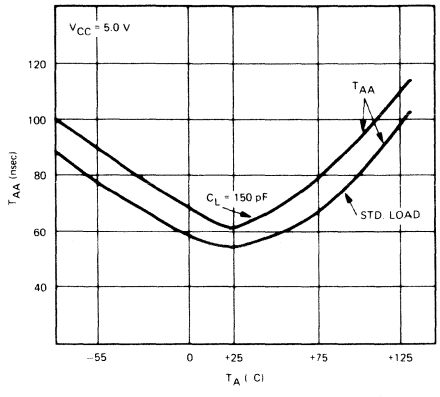
GENERATION OF THE LETTER "F"

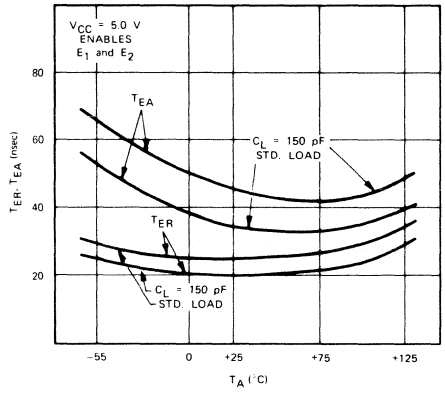


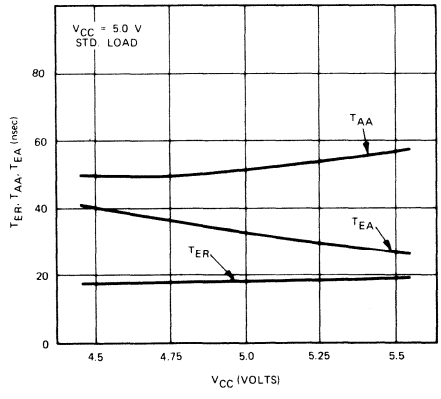
A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

ASCII INPUT ADDRESS	B_5B_4 $A_8A_7A_6$ 000	B_5B_4 $A_8A_7A_6$ 001	B_5B_4 $A_8A_7A_6$ 010	B_5B_4 $A_8A_7A_6$ 011	B_5B_4 $A_8A_7A_6$ 100	B_5B_4 $A_8A_7A_6$ 101	B_5B_4 $A_8A_7A_6$ 110	B_5B_4 $A_8A_7A_6$ 111
$B_3B_2B_1$ $A_5A_4A_3$ 000								
$B_3B_2B_1$ $A_5A_4A_3$ 001								
$B_3B_2B_1$ $A_5A_4A_3$ 010								
$B_3B_2B_1$ $A_5A_4A_3$ 011								
$B_3B_2B_1$ $A_5A_4A_3$ 100								
$B_3B_2B_1$ $A_5A_4A_3$ 101								
$B_3B_2B_1$ $A_5A_4A_3$ 110								
$B_3B_2B_1$ $A_5A_4A_3$ 111								

* These representations were obtained from the USASI X 3.2 Code Practice Manual, Address $A_8 = B_7 = \overline{B_6}$.







CHARACTER GENERATOR OPERATION

The intended application for the MM6074 is the generation of 64 USACII characters utilizing a readout system which generates the characters vertically a 9 bit column at a time. Each 63 bit character is composed of 7 distinct 9 bit lines. One of the 64 characters is selected by the 6 bit address applied to A_3 thru A_8. The particular 9 bit column within each character is determined by the 3 bit address applied to A_0, A_1 and A_2. The binary address 000 on A_0, A_1, and A_2 provides a blank line for character line spacing. The memory is enabled when both E_1 and E_2 are low and E_3 is high.

256-BIT BIPOLAR(256x1) RANDOM ACCESS MEMORY

5530/6530
5531/6531

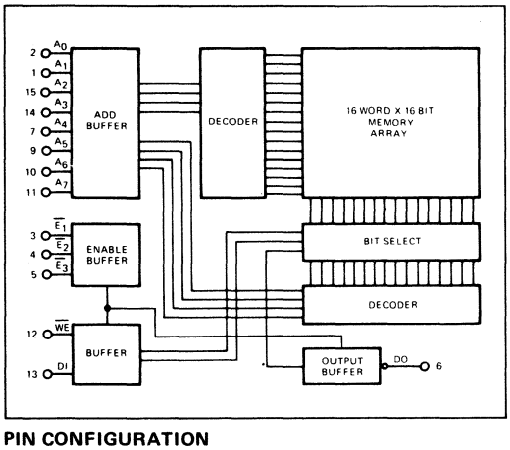
Monolithic Memories
INCORPORATED

PRODUCT FEATURES

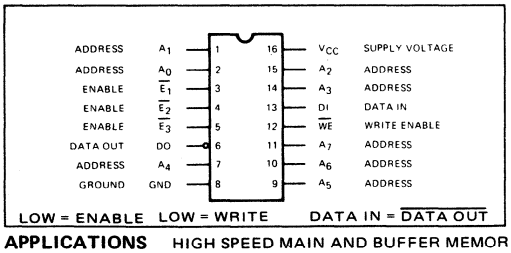
- 55 ns Max. Access Time over 0°C to 75°C and ±5% Voltage Variation (6530/6531)
- 70 ns Max. Access Time over −55°C to 125°C and ±10% Voltage Variation (5530/5531)
- Advanced Schottky Processing
- Low Input Current (250 μA Max.)
- Single Layer Metal for Reliability
- The Data Stored is on the Data Out Pin During a Write Cycle
- Fully Decoded with 3 Chip Enables

	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
6530		X		X
6531		X	X	
5530	X			X
5531	X		X	

LOGIC DIAGRAM



PIN CONFIGURATION

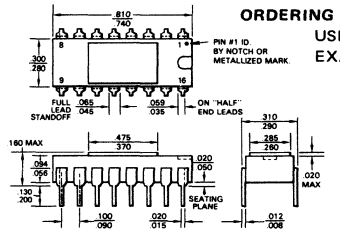


PACKAGE OUTLINE

16 Pin Ceramic (Side Braze)

$\theta_{JA} \approx 68°C/WATT$

SOLDERED TO BOARD IN STILL AIR

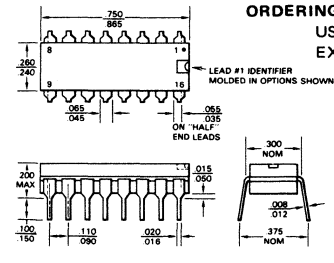


ORDERING INFORMATION
USE NO SUFFIX —
EXAMPLE 6531

16 Pin Plastic

$\theta_{JA} \approx 90°C/WATT$

SOLDERED TO BOARD IN STILL AIR



ORDERING INFORMATION
USE THE SUFFIX N
EXAMPLE 6531 N

APPLICATIONS HIGH SPEED MAIN AND BUFFER MEMORIES

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910—339-9229

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V
Input Voltage	−1.2 to 7.0 V
Output Current	100 mA
Storage Temperature	−65 to 160°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.

D.C. CHARACTERISTICS*

PARAMETER		CONDITIONS	5530/5531			6530/6531			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V			−250			−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			25			25	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 10 mA			0.50				V
		V_{CC} = Min, I_{OL} = 15 mA						0.50	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, All Inputs Open (worst case)		97	135		97	130	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.85			0.85	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max = V_{CEX}			100			100	μA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA			−1.0			−1.0	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz Output in High State		8.0			8.0		pF
THREE STATE PARAMETERS – 5531, 6531 ONLY									
I_{LZ}	Output Leakage High Impedance State	V_O = 0.45 V			−100			−100	μA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5 V	−20		-70	−20		-70	mA
I_{HZ}	Output Leakage High Impedance State	V_{CC} = Max = V_O			100			100	μA
V_{OH}	Output Voltage "High"	I_O = −3.2 mA	2.4			2.4			V

* Unless otherwise indicated, all limits for the 6530/6531 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5530/5531 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C.

1. Typical values are measured at 5.0 V and 25°C.

A.C. CHARACTERISTICS WITH STANDARD LOAD (FIG. 1)

PARAMETER	SYMBOL	FIGURE	5530/5531 5.0 V ± 10%, -55 to 125°C		6530/6531 5.0 V ± 5%, 0 to 75°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	2	20	70	20	55
Enable Access Time	T_{EA}	2	5.0	45	5.0	35
Enable Recovery Time	T_{ER}	2	5.0	35	5.0	35
Write Pulse Width	T_{WP}	3	65		45	
Time Input Data Appears at the Output Following a Write Command $T_{DWO} \geq$ MIN	T_{DW}	3		120		90
Data In and Write Enable Overlap Time	T_{DWO}	3	65		45	
Address to Write Enable Set-up Time		3	0		0	
Address to Write Enable Hold Time		3	0		0	
Chip Enable to Write Enable Set-up Time		3	10		10	
Chip Enable to Write Enable Hold Time		3	0		0	
5531/6531 ONLY						
Chip Enable to Low Impedance Delay	T_{ON}		0		0	
Chip Enable to High Impedance Delay	T_{OFF}			25		25

STANDARD TEST CIRCUIT

STANDARD LOAD

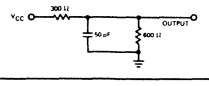
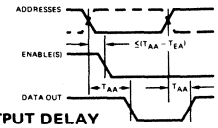


FIGURE 1.

Input Pulse Amplitude = 2.5 V
Input Rise and Fall Time
5.0 ns From 1.0 V to 2.0 V
Measurements Made at 1.50 V

WAVEFORMS

READ CYCLE **ADDRESS TO OUTPUT DELAY**



CHIP ENABLE TO OUTPUT DELAY

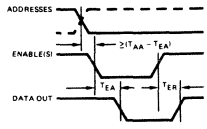


Figure 2

WRITE CYCLE

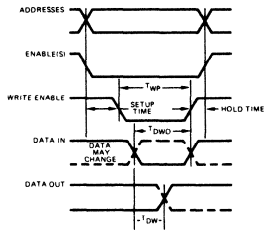


Figure 3

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 15 mA for the 6530
10 mA for the 5530
I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four 6530 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 15 mA

$$R_L(\max) = \frac{V_{CC}-2.40\ V}{M(100\ \mu A)+N(I_R)}$$

$$R_L(\max) = \frac{5.0-2.4\ V}{4\ (100\ \mu A) + 3\ (40\ \mu A)} = 5000 \text{ ohms}$$

$$R_L(\min) = \frac{V_{CC}-0.45\ V}{I_{OL}-N(I_F)}$$

$$R_L(\min) = \frac{5.0-0.45\ V}{15\ mA-3(1.6\ mA)} = 446 \text{ ohms}$$

THREE-STATE OUTPUT – SEE FIGURES A AND B

FIGURE A
THREE-STATE OUTPUT

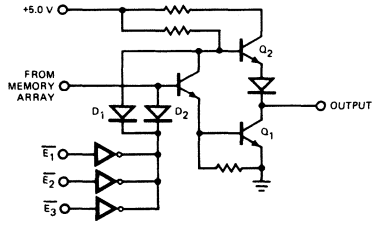
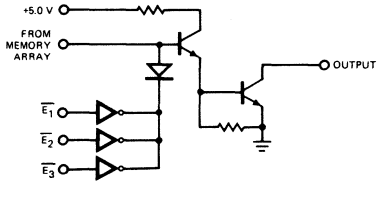


FIGURE B
OPEN COLLECTOR OUTPUT



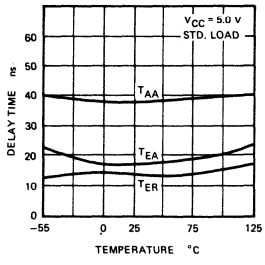
The three-state output of the 5531/6531 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

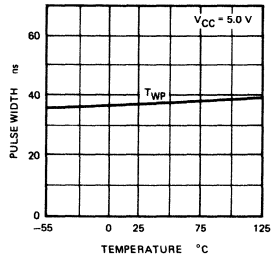
In a system environment, up to 33 memory outputs of the 5531/6531 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

CURVES OF TYPICAL DEVICES

ACCESS TIME



WRITE ENABLE WIDTH VS. TEMPERATURE



TYPICAL I_{CC} IN mA vs. TEMPERATURE AND V_{CC} WITH ALL INPUTS AND OUTPUTS OPEN

	4.50 V	4.75 V	5.00 V	5.25 V	5.50 V
−55°C	86.0	94.0	100.0	108.0	115.0
0°C	86.6	93.7	99.0	107.0	113.5
25°C	86.1	92.8	98.0	105.0	112.0
75°C	83.6	90.3	96.1	101.0	108.0
125°C	81.6	86.0	92.2	96.4	102.0

NOTE: The change in I_{CC} from all inputs open to all inputs grounded is $\leq$ 1.5 mA.

MEMORY OPERATION

READ: The memory is addressed with the $A_0 - A_7$ inputs which selects one of the 256 words. The chip is enabled by making all chip enables low. If any chip enables are high the chip is disabled. If the write enable is HIGH and the chip is enabled the stored data is read out on the data out pin. The data read out is the COMPLEMENT of the data written in during the write cycle.

WRITE: The memory is addressed with the $A_0 - A_7$ inputs which selects one of the 256 words. The chip is enabled as in the read cycle. If the write enable is LOW the data on the data input pin is written into the addressed word. The data out of the memory during the write cycle is the complement of the data written in. This allows checking of the stored data during the write cycle. **Some memory devices may write in as fast as 10 ns** so address and write enable timing must be carefully controlled, when the memory is operated with the enables activated throughout the cycle.

TRUTH TABLE:

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
ALL LOW	LOW	WRITE	COMPLEMENT OF DATA INPUT
ALL LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
ONE OR MORE HIGH	DON'T CARE	HOLD	5531/6531 HIGH IMPEDANCE STATE 5530/6530 HIGH

MEMORY EXPANSION RULES

1. TO EXPAND THE NUMBER OF BITS IN THE WORD:
   Tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
2. TO EXPAND THE NUMBER OF WORDS:
   Tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enables to pick one row of packages.

64-BIT BIPOLAR (16 x 4) RANDOM ACCESS MEMORY

6560/3101A, 6561 5560,5561

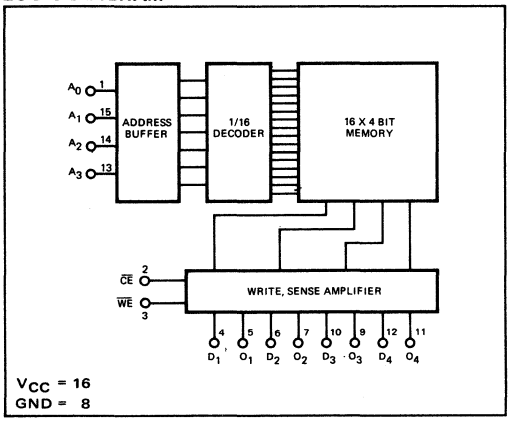
Monolithic Memories
INCORPORATED

PRODUCT FEATURES

- 35 ns Max. Access Time Over 0° C to 75° C and ±5% Voltage Variation (6560/3101A, 6561)
- 60 ns Max Access Time Over −55° C to 125° C and ±10% Voltage Variation (5560/5561)
- Advanced Schottky Processing
- Low Input Current (250 μA Max.)
- Single Layer Metal for Reliability
- Data Outputs Are Off During a Write Cycle
- Fully Decoded and TTL Compatible
- Open Collector or Three State Outputs
- The 6560 is Pin and Performance Compatible With the 3101A

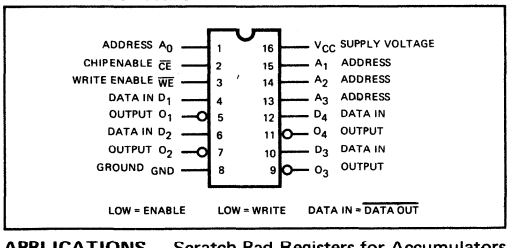
	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
6560/3101A		X		X
6561		X	X	
5560	X			X
5561	X		X	

LOGIC DIAGRAM



V_{CC} = 16
GND = 8

PIN CONFIGURATION



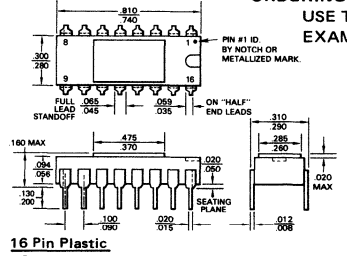
PACKAGE OUTLINE

16 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68° C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20° C/watt

ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE 6560D

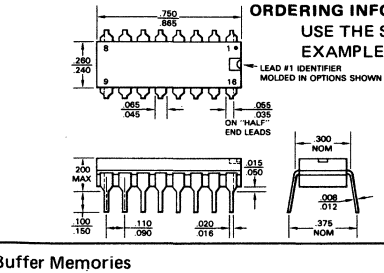


16 Pin Plastic

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 86C/watt

Θ_{JC} (thermal resistance from junction to junction to case with freon as a heat sink) ≈ 36° C/watt

ORDERING INFORMATION
USE THE SUFFIX N
EXAMPLE 6560N



APPLICATIONS Scratch Pad Registers for Accumulators and Buffer Memories

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

SEPTEMBER 1973

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7.0 V
Input Voltage	−0.5 to 5.5 V
DC Input Current	−25 to 5.0 mA
Output Current	100 mA
Storage Temperature	−65 to 160°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.
Functional operation at these limits is not guaranteed or implied.

D.C. CHARACTERISTICS:

Unless otherwise indicated, all limits for the 6560/6561 are guaranteed for 5.0 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5560/5561 are guaranteed for 5.0 V ±10% in a free air temperature of −55 to 125°C.

PARAMETER		CONDITIONS		5560/5561			6560/6561			UNITS
				MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V			−40	−250		−40	−250	µA
I_F	Input Leakage Current. All Inputs	V_{CC} = Max, V_R = 2.40 V				25			25	µA
I_{RB}	Input Leakage Current. All Inputs	V_{CC} = Max, V_{RB} = 5.50 V				1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 15 mA				0.50			0.50	V
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs GRD and Outputs Open	5560/6560		70	105		70	105	mA
			5561/6561		75	125		75	125	
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V				0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V		2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.40 V				100			100	µA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA				−1.0			−1.0	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1.0 MHz			7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1.0 MHz Output in High State			8.0			8.0		pF
THREE STATE PARAMETERS — 5561/6561 ONLY										
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5.0 V		−20	−50	−90	−20	−50	−90	mA
I_{HZ}	Output Leakage High Impedance State	V_{CC} = Max, V_O = .45 to 2.40 V				±100			±100	µA
V_{OH}	Output Voltage HIGH	I_O = −3.2 mA		2.4	3.4		2.4	3.4		V

1. Typical values are measured at 5.0 V and 25°C.

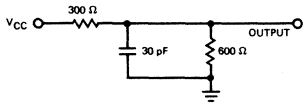
A.C. CHARACTERISTICS With Standard Load (Fig. 1)

PARAMETER	SYMBOL	FIGURE	5560/5561 5.0 V ± 10%, −55 to 125°C		6560/6561 5.0 V ± 5%, 0 to 75°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	2	10	60	10	35
Enable Access Time	T_{EA}	2	5.0	35	5.0	25
Enable Recovery Time	T_{ER}	2	5.0	35	5.0	25
Write Pulse Width	T_{WP}	3	40		25	
Write Enable to Output High Time	T_{WH}	3		25		25
Data In and Write Enable Overlap Time	T_{DWO}	3	40		25	
Address to Write Enable Set-up Time		3	0		0	
Address to Write Enable Hold Time		3	0		0	
Chip Enable to Write Enable Set-up Time		3	10		10	
Chip Enable to Write Enable Hold Time		3	0		0	
5561/6561 ONLY						
Chip Enable to Low Impedance Delay	T_{ON}		5		5	
Chip Enable to High Impedance Delay	T_{OFF}			30		20

ELECTRICAL PARAMETERS

STANDARD TEST CIRCUIT

STANDARD LOAD



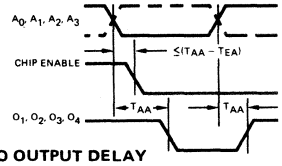
Input Pulse Amplitude = 2.5 V
Input Rise and Fall Time
5.0 ns From 1.0 V to 2.0 V
Measurements Made at 1.50 V

Figure 1

WAVEFORMS

READ CYCLE

ADDRESS TO OUTPUT DELAY



CHIP ENABLE TO OUTPUT DELAY

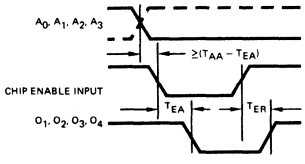


Figure 2

WRITE CYCLE

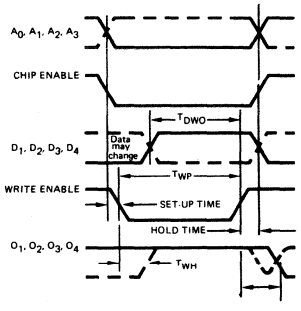


Figure 3

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 15 mA for the 6560 and 5560

I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four 6560 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven to find the range of permissible pullup resistors at V_{CC} = 5.0 V.

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 15 mA

$$R_L(\max) = \frac{V_{CC}-2.40\ V}{M(100\ \mu A)+N(I_R)} \qquad R_L(\max) = \frac{5.0-2.4\ V}{4(100\ \mu A)+3\ (40\ \mu A)} = 5000 \text{ ohms}$$

$$R_L(\min) = \frac{V_{CC}-0.45\ V}{I_{OL}-N(I_F)} \qquad R_L(\min) = \frac{5.0-0.45\ V}{15\ mA-3(1.6\ mA)} = 446 \text{ ohms}$$

MEMORY CHARACTERISTICS

THREE-STATE OUTPUT – See Figures A and B

FIGURE A
THREE-STATE OUTPUT

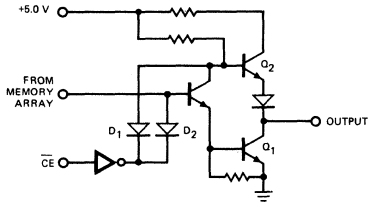
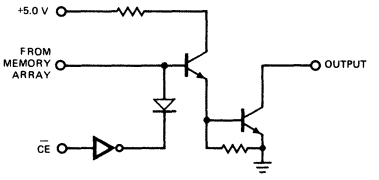


FIGURE B
OPEN COLLECTOR OUTPUT



The three-state output of the 5561/6561 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment, up to 33 memory outputs of the 5561/6561 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise probelms could result.

OPERATION — EXPANSION RULES

MEMORY OPERATION

READ: The memory is addressed with the $A_0 - A_3$ inputs which selects one of the 16 words. The chip is enabled by making the chip enable LOW. If the chip enable is HIGH the chip is disabled. If the write enable is HIGH and the chip is enabled the stored data is read out on the data out pin. The data read out is the COMPLEMENT of the data written in during the write cycle.

WRITE: The memory is addressed with the $A_0 - A_3$ inputs which selects one of the 16 4-bit words. The chip is enabled as in the read cycle. If the write enable is LOW the data on the data input pin is written into the addressed word. The data out pins of the memory during the write cycle will be kept OFF in the case of the 5560/6560 and in the third state (high impedance state) for the 5561/6561, by control of internal circuitry. Some memory devices may write in as fast as 10 ns so address and write enable timing must be carefully controlled, when the memory is operated with the enable activated throughout the cycle.

TRUTH TABLE:

CHIP ENABLE	WRITE ENABLE	OPERATION	DATA OUTPUTS	
LOW	LOW	WRITE	5560/6560	OFF
			5561/6561	HIGH IMPEDANCE STATE
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA	
HIGH	DON'T CARE	HOLD	5560/6560	OFF
			5561/6561	HIGH IMPEDANCE STATE

MEMORY EXPANSION RULES

1. TO EXPAND THE NUMBER OF BITS IN THE WORD:
   Tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
2. TO EXPAND THE NUMBER OF WORDS:
   Tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enable to pick one row of packages.

LOW POWER 256-BIT BIPOLAR (256 x 1) RANDOM ACCESS MEMORY

L5530/L6530 L5531/L6531

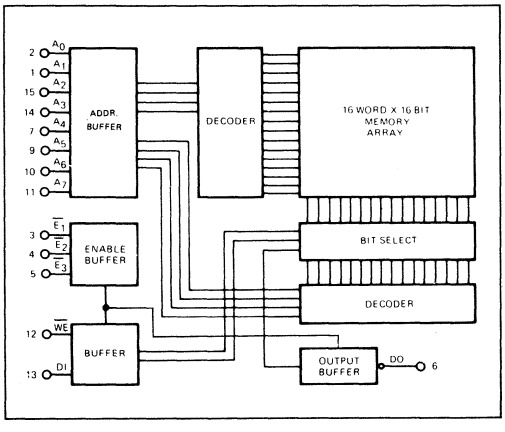
Monolithic Memories
INCORPORATED

PRODUCT FEATURES

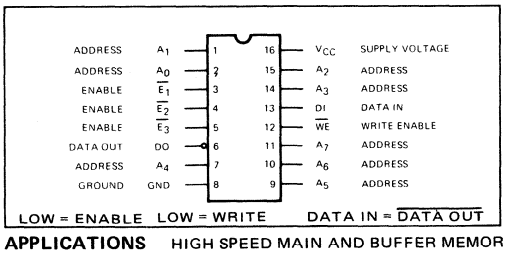
- Typical Power Dissipation of 275 mW
- 115 ns Max. Access Time over 0°C to 75°C and ±5% Voltage Variation (L6530/L6531)
- 130 ns Max. Access Time over −55°C to 125°C and ±10% Voltage Variation (L5530/L5531)
- Advanced Schottky Processing
- Low Input Current (125 μA Max.)
- Single Layer Metal for Reliability
- The Data Stored is on the Data Out Pin During a Write Cycle
- Fully Decoded with 3 Chip Enables

	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
L6530		X		X
L6531		X	X	
L5530	X			X
L5531	X		X	

LOGIC DIAGRAM



PIN CONFIGURATION



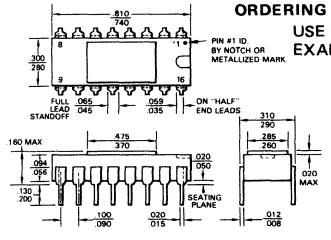
APPLICATIONS HIGH SPEED MAIN AND BUFFER MEMORIES

PACKAGE OUTLINE

16 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 24°C/watt

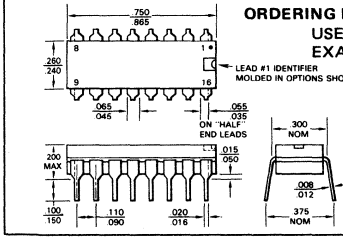


ORDERING INFORMATION
USE NO SUFFIX—
EXAMPLE L6530D

16 Pin Plastic

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 90°C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 36°C/watt



ORDERING INFORMATION
USE THE SUFFIX N
EXAMPLE L6530N

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910—339-9229

MARCH 1974

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V
Input Voltage	−1.2 to 7.0 V
Output Current	100 mA
Storage Temperature	−65 to 160°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.

D.C. CHARACTERISTICS:

Unless otherwise indicated, all limits for the L6530/L6531 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the L5530/L5531 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C.

PARAMETER		CONDITIONS	L5530/L5531			L6530/L6531			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All inputs	V_{CC} = Max, V_F = 0.45 V			-125			-125	µA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			25			25	µA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5 V			1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 10 mA		0.35	0.50				V
		V_{CC} = Min, I_{OL} = 15 mA					0.35	0.50	V
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs at 2.4 V, All Outputs Open		55	85		55	75	mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.40 V			100			100	µA
	High Stored or Disabled	V_{CC} = Max = V_{CEX}			1			1	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5 mA		1.0	-1.5		-1.0	-1.5	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz, Output in High State		8.0			8.0		pF
THREE STATE PARAMETERS — L5531/L6531 ONLY									
I_{LZ}	Output Leakage, High Impedance State	V_O = 0.45 V			−100			−100	µA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5 V	−20		−70	−20		-70	mA
I_{HZ}	Output Leakage, High Impedance State	V_{CC} = Max, V_O = 2.4V			100			100	µA
V_{OH}	Output Voltage "High"	I_O = −3.2 mA	2.4			2.4			V

1. Typical values are measured at 5.0 V and 25°C.

A.C. CHARACTERISTICS WITH STANDARD LOAD (FIG. 1)

PARAMETER	SYMBOL	FIGURE	L5530/L5531 5.0 V ± 10%, -55 to 125°C		L6530/L6531 5.0 V ± 5%, 0 to 75°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
Address Access Time	T_{AA}	2	20	130	20	115
Enable Access Time	T_{EA}	2	5.0	80	5.0	60
Enable Recovery Time	T_{ER}	2	5.0	85	5.0	60
Write Pulse Width	T_{WP}	3	100		85	
Time Input Data Appears at the Output Following a Write Command $T_{DWO} \geq$ MIN	T_D AND T_{DW}	3		130		110
Data In and Write Enable Overlap Time	T_{DWO}	3	100		85	
Address to Write Enable Set-up Time		3	0		0	
Address to Write Enable Hold Time		3	0		0	
Chip Enable to Write Enable Set-up Time		3	10		10	
Chip Enable to Write Enable Hold Time		3	0		0	
5531/6531 ONLY						
Chip Enable to Low Impedance Delay	T_{ON}		0		0	
Chip Enable to High Impedance Delay	T_{OFF}			80		55

STANDARD TEST CIRCUIT

STANDARD LOAD

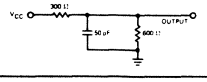


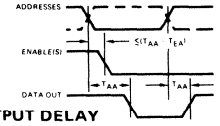
FIGURE 1.

Input Pulse Amplitude = 2.5 V
Input Rise and Fall Time
5.0 ns From 1.0 V to 2.0 V
Measurements Made at 1.50 V

ELECTRICAL PARAMETERS

WAVEFORMS

READ CYCLE — **ADDRESS TO OUTPUT DELAY**



CHIP ENABLE TO OUTPUT DELAY

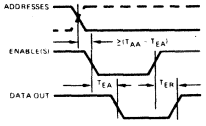


Figure 2

WRITE CYCLE

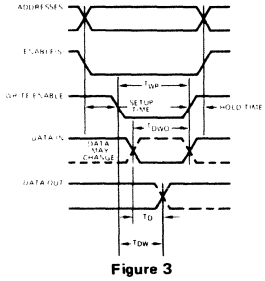


Figure 3

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value

N = The number of TTL loads the memory must drive

M = The number of memory packages wire OR'ed

I_{OL} = 15 mA for the L6530
10 mA for the L5530

I_F = The maximum input load current of the TTL family at 0.45 V

I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four L6530 memory packages are wire OR'ed and 3 Series 74 TTL gates must be driven find the range of permissible pullup resistors at V_{CC} = 5.0 V.

M = 4
N = 3
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 15 mA

$$R_L(\max) = \frac{V_{CC}-2.40\ V}{M(100\ \mu A)+N(I_R)} \qquad R_L(\max) = \frac{5.0-2.4\ V}{4\ (100\ \mu A) + 3\ (40\ \mu A)} = 5000 \text{ ohms}$$

$$R_L(\min) = \frac{V_{CC}-0.45\ V}{I_{OL}-N(I_F)} \qquad R_L(\min) = \frac{5.0-0.45\ V}{15\ mA-3(1.6\ mA)} = 446 \text{ ohms}$$

THREE-STATE OUTPUT – SEE FIGURES A AND B

FIGURE A
THREE-STATE OUTPUT

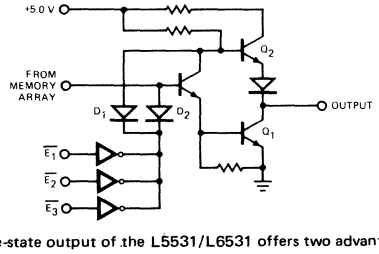
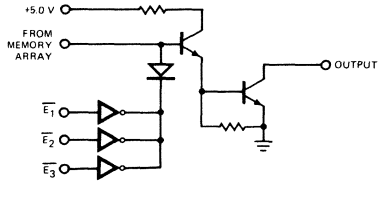


FIGURE B
OPEN COLLECTOR OUTPUT



The three-state output of the L5531/L6531 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

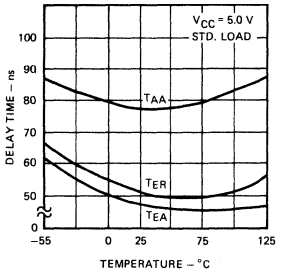
When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment, up to 33 memory outputs of the L5531/L6531 can be connected to a common bus. All of the devices except one are placed in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

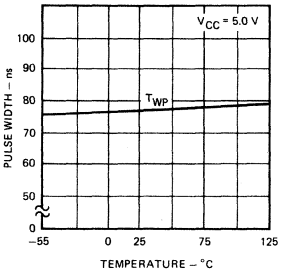
MEMORY CHARACTERISTICS

CURVES OF TYPICAL DEVICES

ACCESS TIME



WRITE ENABLE WIDTH VS. TEMPERATURE



TYPICAL I_{CC} IN mA vs. TEMPERATURE AND V_{CC} WITH ALL INPUTS AND OUTPUTS OPEN

	4.50 V	4.75 V	5.00 V	5.25 V	5.50 V
–55°C	47	51	56	60	69
0°C	46	50	54	57	61
25°C	45	48	52	55	50
75°C	42	44	47	50	53
125°C	39	41	44	46	49

NOTE: The change in I_{CC} from all inputs open to all inputs grounded is $\leq$ 1.5 mA.

MEMORY OPERATION

READ: The memory is addressed with the $A_0 - A_7$ inputs which selects one of the 256 words. The chip is enabled by making all chip enables low. If any chip enables are high the chip is disabled. If the write enable is HIGH and the chip is enabled the stored data is read out on the data out pin. The data read out is the COMPLEMENT of the data written in during the write cycle.

WRITE: The memory is addressed with the $A_0 - A_7$ inputs which selects one of the 256 words. The chip is enabled as in the read cycle. If the write enable is LOW the data on the data input pin is written into the addressed word. The data out of the memory during the write cycle is the complement of the data written in. This allows checking of the stored data during the write cycle. **Some memory devices may write in as fast as 10 ns** so address and write enable timing must be carefully controlled, when the memory is operated with the enables activated throughout the cycle.

TRUTH TABLE:

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT	
ALL LOW	LOW	WRITE	COMPLEMENT OF DATA INPUT	
ALL LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA	
ONE OR MORE HIGH	DON'T CARE	HOLD	L5531/L6531	HIGH IMPEDANCE STATE
			L5530/L6530	OFF

MEMORY EXPANSION RULES

1. TO EXPAND THE NUMBER OF BITS IN THE WORD:
   Tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
2. TO EXPAND THE NUMBER OF WORDS:
   Tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enables to pick one row of packages.

LOW POWER 64-BIT BIPOLAR (16×4) RANDOM ACCESS MEMORY

L6560/31L01, L6561 L5560, L5561

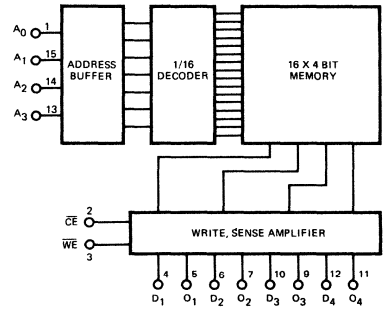
Monolithic Memories INCORPORATED

PRODUCT FEATURES

- Typical Power Dissipation of 125 mW
- 80 n Max. Access Time Over 0°C to 75°C and ±5% Voltage Variation (L6560/31L01, L6561)
- 100 ns Max Access Time Over -55°C to 125°C and ±10% Voltage Variation (L5560, L5561)
- Low Input Current (125 μA Max.)
- Single Layer Metal for Reliability
- Open Collector or Three State Outputs
- The L6560 is Pin and Performance Compatible With the 31L01

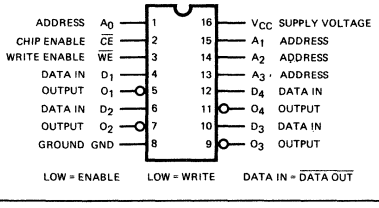
	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
L6560/31L01		X		X
L6561		X	X	
L5560	X			X
L5561	X		X	

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8

PIN CONFIGURATION



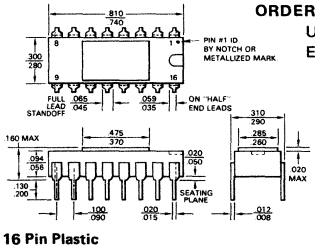
PACKAGE OUTLINE

16 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt

ORDERING INFORMATION
USE THE SUFFIX D
EXAMPLE L6560D

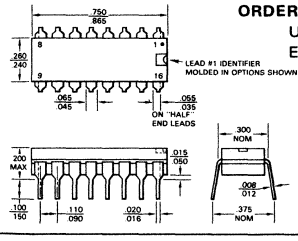


16 Pin Plastic

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 86°C/watt

Θ_{JC} (thermal resistance from junction to junction to case with freon as a heat sink) ≈ 36°C/watt

ORDERING INFORMATION
USE THIS SUFFIX N
EXAMPLE L6560N



Monolithic Memories
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1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

MARCH 1974

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7.0 V
Input Voltage	−0.5 to 5.5 V
DC Input Current	−25 to 5.0 mA
Output Current	100 mA
Storage Temperature	−65 to 160°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.
Functional operation at these limits is not guaranteed or implied.

D.C. CHARACTERISTICS:

Unless otherwise indicated, all limits for the L6560/L6561 are guaranteed for 5.0 V ±5% in a free air temperature of 0 to 75°C; all limits for the L5560/L5561 are guaranteed for 5.0 V ±10% in a free air temperature of −55 to 125°C.

PARAMETER		CONDITIONS		L5560/L5561			L6560/L6561			UNITS
				MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V				−125			−125	μA
I_F	Input Leakage Current. All Inputs	V_{CC} = Max, V_R = 2.40 V				25			25	μA
I_{RB}	Input Leakage Current. All Inputs	V_{CC} = Max, V_{RB} = 5.50 V				1			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 4.8 mA				0.50			0.50	V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, Inputs GRD and Outputs Open	L5560/L6560		25	45		25	40	mA
			L5561/L6561		25	45		25	40	
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V				0.80			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V		2.0			2.0			V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.40 V				100			100	μA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −5.0 mA				−1.0			−1.0	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1.0 MHz			7.0			7.0		pF
C_O	Output Capacitance	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1.0 MHz Output in High State			8.0			8.0		pF
THREE STATE PARAMETERS — L5561/L6561 ONLY										
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = 5.0 V		−20	−50	−90	−20	−50	−90	mA
I_{HZ}	Output Leakage High Impedance State	V_{CC} = Max, V_O = .45 to 2.40 V				±100			±100	μA
V_{OH}	Output Voltage HIGH	I_O = −1.6 mA		2.4	3.4		2.4	3.4		V

NOTE:
1. Typical values are measured at 5.0 V and 25°C.

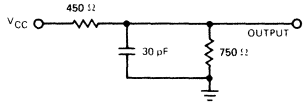
A.C. CHARACTERISTICS With Standard Load (Fig. 1)

PARAMETER	SYMBOL	FIGURE	L5560/L5561 5.0 V ± 10%, −55 to 125°C		L6560/L6561 5.0 V ± 5%, 0 to 75°C	
			MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ps)
Address Access Time	T_{AA}	2	20	100	20	80
Enable Access Time	T_{EA}	2	10	80	10	60
Enable Recovery Time	T_{ER}	2	10	80	10	60
Write Pulse Width	T_{WP}	3	100		80	
Data In and Write Enable Overlap Time	T_{DWO}	3	100		80	
Address to Write Enable Set-up Time		3	0		0	
Address to Write Enable Hold Time		3	0		0	
Chip Enable to Write Enable Set-up Time		3	10		10	
Chip Enable to Write Enable Hold Time		3	0		0	
L5561/L6561						
Chip Enable to Low Impedance Delay	T_{ON}		5		5	
Chip Enable to High Impedance Delay	T_{OFF}			75		55

ELECTRICAL PARAMETERS

STANDARD TEST CIRCUIT

STANDARD LOAD



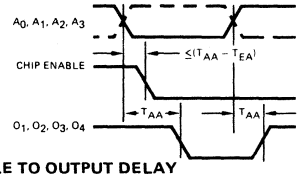
Input Pulse Amplitude = 2.5 V
Input Rise and Fall Time
5.0 ns From 1.0 V to 2.0 V
Measurements Made at 1.50 V

Figure 1

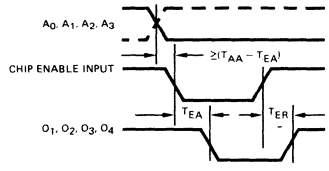
WAVEFORMS

READ CYCLE

ADDRESS TO OUTPUT DELAY



CHIP ENABLE TO OUTPUT DELAY



WRITE CYCLE

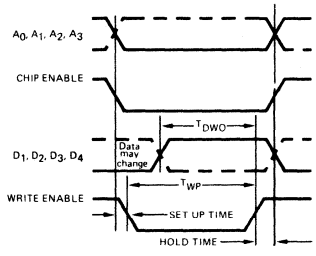


Figure 3

PULLUP RESISTOR SELECTION FOR OPEN COLLECTOR OUTPUTS

LET R_L = Pullup resistor value
N = The number of TTL loads the memory must drive
M = The number of memory packages wire OR'ed
I_{OL} = 4.8 mA for the L6560 and L5560

I_F = The maximum input load current of the TTL family at 0.45 V
I_R = The maximum leakage current of the TTL family at 2.40 V

TTL Series	I_F	I_R
74	1.6 mA	40 μA
74L	0.16 mA	10 μA
74H, 74S	2.0 mA	50 μA

Example:
Four L6560 memory packages are wire OR'ed and 1 Series 74 TTL gate must be driven to find the range of permissible pullup resistors at V_{CC} = 5.0 V.

M = 4
N = 1
I_F = 1.6 mA
I_R = 40 μA
I_{OL} = 4.8 mA

$$R_L(\max) = \frac{V_{CC} - 2.40\ V}{M(100\ \mu A) + N(I_R)}$$

$$R_L(\max) = \frac{5.0 - 2.4}{4(100\ \mu A) + 1\ (40\ \mu A)} = 5910 \text{ ohms}$$

$$R_L(\min) = \frac{V_{CC} - 0.45\ V}{I_{OL} - N(I_F)}$$

$$R_L(\min) = \frac{5.0 - 0.45}{4.8\ mA - 1(1.6\ mA)} = 1197 \text{ ohms}$$

MEMORY CHARACTERISTICS

THREE-STATE OUTPUT – See Figures A and B

FIGURE A
THREE-STATE OUTPUT

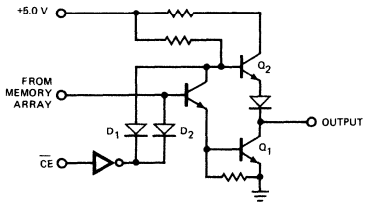
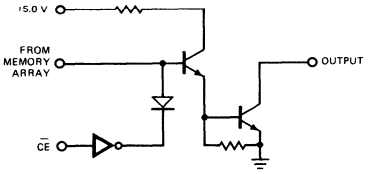


FIGURE B
OPEN COLLECTOR OUTPUT



The three-state output of the L5561/L6561 offers two advantages over open collector types. The first advantage is that a low impedance driver Q_2 is available for driving capacitance on the memory output resulting in faster low to high transitions and the second advantage is that no pullup resistor is required.

When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance third state.

In a system environment, up to 33 memory outputs of the L5561/L6561 can be connected to a common bus. All of the devices except one are place in the high impedance state and the selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device. While physical damage to the device under these circumstances is unlikely, system noise problems could result.

OPERATION – EXPANSION RULES

MEMORY OPERATION

READ: The memory is addressed with the $A_0 - A_3$ inputs which selects one of the 16 words. The chip is enabled by making the chip enable LOW. If the chip enable is HIGH the chip is disabled. If the write enable is HIGH and the chip is enabled the stored data is read out on the data out pin. The data read out is the COMPLEMENT of the data written in during the write cycle.

WRITE: The memory is addressed with the $A_0 - A_3$ inputs which selects one of the 16, 4-bit words. The chip is enabled as in the read cycle. If the write enable is LOW the data on the data input pin is written into the addressed word. The data out pins of the memory during the write cycle will be the complement of the data inputs for the L5560/L6560 (assuming a pullup resistor is attached) and in the third state (high impedance state) for the L5561/L6561. Some memory devices may write in as fast as 15 ns so address and write enable timing must be carefully controlled, when the memory is operated with the enable activated throughout the cycle.

TRUTH TABLE:

CHIP ENABLE	WRITE ENABLE	OPERATION	DATA OUTPUTS	
LOW	LOW	WRITE	L5560/L6560	
			L5561/L6561	HIGH IMPEDANCE STATE
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA	
HIGH	DON'T CARE	HOLD	L5560/L6560	OFF
			L5561/L6561	HIGH IMPEDANCE STATE

MEMORY EXPANSION RULES

1. TO EXPAND THE NUMBER OF BITS IN THE WORD:
   Tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
2. TO EXPAND THE NUMBER OF WORDS:
   Tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enable to pick one row of packages.

4-BIT EXPANDABLE BIPOLAR MICROCONTROLLER

5701/6701

Monolithic Memories
INCORPORATED

	MILITARY	COMMERCIAL
5701	X	
6701		X

PRODUCT FEATURES

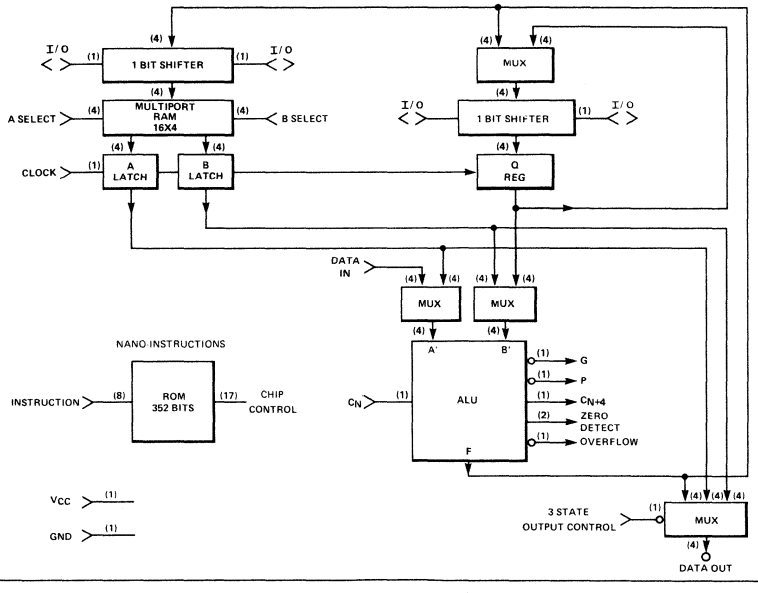
- Complete 4-Bit Bipolar LSI Processor Slice on a Single Chip.
- Replaces 25 TTL MSI Packages and Saves 5.5 Watts.
- 1000 Gate Complexity Schottky LSI - Single Layer Metal.
- 36 Instructions - Arithmetic, Logic, and Shifting Capability with Overflow Detection. Active High or Active Low Logic.
- 16 Directly Addressable, Two-port, General Purpose Accumulators - Full 2 Address Capability, Some 3 Register Operations.
- A Separate Q-Register Useful as a Scratchpad or Accumulator Extension. Direct Data in and Accumulator Operations.
- Separate Low Fan in Input Bus and 3 State Output Bus.
- Expandable to handle N Bit Words with Full Carry Look-ahead.
- 200 ns Cycle (6701) which can Perform Multiple Nano-instructions such as Subtract, Shift, and Store in One Cycle.

APPLICATIONS

- The Ideal Product for Upgrading or Replacing Existing Central Processing Units and Maintaining the Existing Software. The 5701/6701 can be Microprogrammed to Efficiently Emulate (Simulate) Most Machines.
- Hard Wired Controllers - Tape and Disk Controllers - Data Concentrators.
- Point of Sale Terminals, Special Purpose Processors.
- Process and Machine Control.
- Word Processing and Navigation Systems.
- Intelligent Terminals and Game Machines.
- Traffic Control and Communications Systems.
- Upgrade Systems using the 74181, 9340, 9341, 74S281 Arithmetic Logic Units.

BLOCK DIAGRAM – 5701/6701

NOTE: THE NUMBERS IN PARENTHESES ARE THE NUMBER OF SIGNAL LINES.



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AUGUST 1974

I. INTRODUCTION

A) GENERAL DESCRIPTION

The microcontroller is designed to be used as a 4-bit processor slice of a conventional central processing unit (C.P.U) It can also be used in peripheral controllers, (tape, disk, etc.,) or as the heart of a microprocessor, terminal, or computer. It is a single chip 1000 gate complexity bipolar LSI device.

The two address capability (ability to work on two accumulators at once) and the powerful nano-instructions permit design of sub 1 microsecond cycle time hard wired C.P.U.'s or efficient emulation (imitation) of conventional machines using off chip ROMs for microprogramming.

The microcontroller will handle the data flow section of most computers since it is expandable to handle any word length in increments of 4 bits without significant speed degradation (look-ahead outputs are available). The 16 on-chip general purpose accumulators give the microcontroller the type of C.P.U. usually found only in high performance top of the line 16-bit minicomputers or 24 or 32-bit computers. It can be thought of as a general purpose 4-bit register and arithmetic logic unit with a separate A operand, B operand, data-in, and data-out ports. Additional accumulators or registers if required can be added with off chip packages tied to the microcontrollers data in pins.

B) TTL EQUIVALENT

The microcontroller is similar in function to the 25 TTL MSI packages listed below. It saves 375 I/O pins, 5.6 watts and 30 square inches of board area.

Function	TTL #	#14 Pin or #16 Pin Pkgs.	#24 Pin Pkgs.	Advertised Gate Complexity (Each Pkg.)	Gate Complexity Total	Typical Power Each (Watts)	Total Power (Watts)
32 x 9 & 8 x 8 ROMs	7488	3		70	210	.50	1.50
16 x 4 Multiport RAM	74172		4	110*	440	.56	2.24
Arithmetic Logic Unit	74181		1	75	75	.55	.55
Storage Latches	7475	2		28	56	.16	.32
J-K Flip Flop (Q Reg)	74107	2		22	44	.10	.20
4 to 1 MUX	74153	6		16	96	.20	1.20
O/I True Complement	74H87	2		18	36	.27	.54
Dual 4 Bit Select	74157	2		15	30	.15	.30
Quad 2 to 1 MUX with 3 State Outputs	74S257	2		15	30	.30	.60
3 State Buffer	DM8094	1		5	5	.18	.18
Totals		20	5		1022		6.63

*NOTE: The 74172 is advertised at 201 gate complexity but we are using only 2 of the 3 address capability, hence we have counted it as 110 gates.

TABLE 1

C) PROCESS AND PACKAGING

The microcontroller is manufactured by an advanced Schottky bipolar single layer metal process. The chip requires only 5 volts and ground and all inputs and outputs are totally TTL compatible. The chip is packaged in a standard 40-pin dual in-line ceramic package.

D) POWER

The chip is designed to dissipate maximum power at low temperature. The power is minimum at high temperature. This feature permits full military range parts and easier power supply design.

E) PERFORMANCE

The microcontroller can execute one instruction every 200ns (250ns for the 5701). The instructions are more complex than normal micro-instructions permitting multiple operations in one cycle without timing problems.

II. OPERATION

A) BLOCK DIAGRAM

A detailed block diagram of the chip is shown in Figure 1. Note the legend used in the upper left hand corner for package inputs and outputs. The logic and control lines are shown as they are implemented on the chip even though fewer control inputs might be required by discrete logic devices. The dual 4-bit selects, at the input to the arithmetic logic unit, for example, have two "S" input control lines rather than the 74157 TTL equivalent which has one control line for letting through the left four bits or the right four bits on the output 4 bits.

B) ROM (LOWER LEFT CORNER)

Two on chip ROMs (352 bits total) are used to translate the eight (8) instruction lines I_0 to I_7 into 17 on chip control lines (labeled S_1 through S_{17}) which open and close data paths required to execute an instruction.

The microcontroller is offered with a standard instruction set but the on chip ROM's can be custom coded for special customer requirements. (Contact factory for details.)

C) MULTIPORT RAM (UPPER LEFT CORNER)

A 16 word by 4 bit multiple port memory is used to fetch two operands at the same time since the RAM is double decoded (4 A address pins and 4B address pins). We could, for example, read from 0101 on the A address (file #5) and read from 0001 on the B address (file #1) at the same time. The B side of the RAM can be read out or written into independent of the address on the A side. The A side can only be read. The RAM must be loaded via the B side. The RAM if it is enabled is loaded when the clock is low. The duration of time the clock is low is the write enable pulse width required to switch the RAM.

D) LATCHES (CENTER LEFT)

The latches on the RAM outputs are the zero delay type (like 7475) which let the data into the latches appear on the latch outputs until the clock goes low and then hold the data. The latches permit parallel accessing of the RAM and ROM without two delays (one for the ROM and one for the RAM), since the access time of the ROM is masked by the delay through the RAM. The latches eliminate race conditions when the RAM data is fetched and updated in one cycle.

E) ARITHMETIC LOGIC UNIT (LOWER CENTER)

Input multiplexers into the arithmetic logic unit (A.L.U.) under ROM control permit the entry of data in or the A channel of the RAM into the A port of the ALU, and the B channel of the RAM or the Q register into the B port of the ALU.

The ALU is of the conventional type except 0/1 true complement elements have been put in the input ports permitting the realization of a totally symmetrical ALU(i.e., A minus B or B minus A). Overflow detection and two zero detect pin (one for positive and one for negative logic) are also included.

F) OUTPUT MULTIPLEXERS (LOWER RIGHT HAND CORNER)

The 3 to 1 output multiplexers under ROM control let through the ALU output, the A latch output, the B latch output on the data out pins. The output multiplexers are three-state outputs controlled by the three-state output control pin. The three-state outputs permit processing to be performed in the microcontroller without tying up the data out bus.

G) SHIFT MULTIPLEXERS (UPPER LEFT AND UPPER RIGHT)

The four 3 to 1 mux's on top of the Q register permit the ALU output bus F to transfer straight through into the Q register or be shifted 1 bit left or right before being entered into the Q register. The four 3 to 1 multiplexer above the RAM function in the same manner. Both the RAM shifter and the Q shifter employ bi-directional shift in/shift out pins to permit expansion to more than 4 bits.

H) Q REGISTER (UPPER RIGHT)

The Q register can function as an accumulator extension register. It would normally be used to hold the least significant half of the double length product of a multiplication or as a storage register to catch the bits shifted off the beginning or end of a word during left or right shifting. In this mode of operation, the shift out pin of the least significant bit of the RAM shifter would be tied to the shift in pin of the most significant bit of the Q register. The Q register can shift on itself and be loaded from the ALU bus while any instruction is being executed. Its shift control pins, are in common with RAM shift controls permitting RAM shifting into Q and vice versa in one cycle. It can also be used as a program counter or scratchpad.

The Q register is a master slave flip-flop. Data is loaded into the master when the clock goes low (assuming it is enabled by the ROM) and transferred from the master to the slave when the clock goes high.

EXPANDABLE 4 BIT SLICE — 40 PIN PKG.

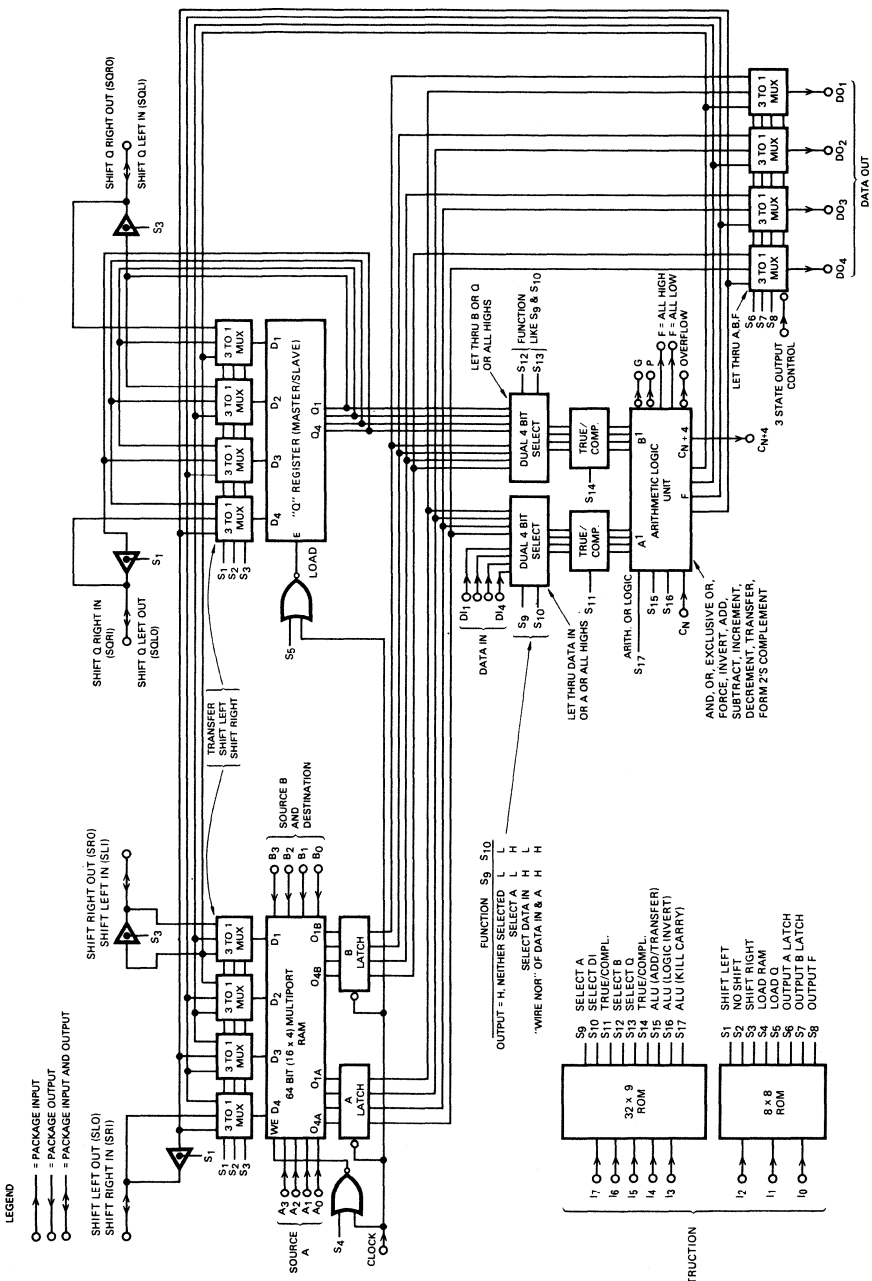


FIGURE 1

III. STATE OF THE ART ALU'S

A comparsion of the 6701 with commercially available ALU's is shown in table 2.

TABLE 2 - 4 BIT ARITHMETIC UNITS

	Arithmetic Logic Unit 74S181	Monolithic Accumulator 74S281	Microcontroller 6701
Year Introduced	**1972**	**1973**	**1974**
Gate Complexity	75	125	1000
Package Size	16 Pin	24 Pin	40 Pin
Number of Accumulators	0	1	16
Multiport Accumulators	No	No	Yes
Number of Useful Arithmetic Instructions	4	11	21
Number of Useful Logic Instructions	10	11	15
One Bit Bidirectional Shift Capability	No	Yes	Yes
Interface to 74S182 Look Ahead Carry Generator	Yes	Yes	Yes
Simultaneous Entry of Two Operands	Yes	No	Yes
Three State Outputs	No	No	Yes
Zero Detect	Yes	No	Yes
Overflow Detection	No	No	Yes
Accumulator Extension Register	No	No	Yes
Accumulator Extension Register One Bit Shift Capability	No	No	Yes
Operate on 3 Registers in One Cycle	NA	No	Yes
Symmetrical ALU (i.e. A minus B and B minus A)	No	Yes	Yes
Number of ALU input ports	2	2	4
Number of ALU output ports	1	1	3
Power Dissipation (TYP)	600 mW	750 mW	900 mW
Power (mW) per Gate	8	6	9
ALU Time Required to Add Two 4 Bit Operands and Store the Result in an Accumulator Inside the ALU. A CPU with 3 to 16 Registers is Assumed	NA	205 ns (Max @ 5.0 V, 25°C) Requires Off Chip 35 ns 64 Bit (16 x 4) RAM	200 ns (Max @ 5.0 V ± 5% 0 to 75°C)
Number of Microcycles Required to Add Two 4 Bit Operands, Store the Result in an Accumulator and Look at the Result	NA	4	1

IV. CPU'S LARGER THAN 4 BITS

CPU's larger than 4 bits will have to wait for the carry generated by an off chip look ahead 74S182 or the ripple carry generated by the lower order package's C_{N+4}. As a result the minimum cycle time of the 5701/6701 will increase. When drawing timing diagram for these CPU's the amount of time the clock is high (T_{CS} of Figure 5) should be increased to permit a longer time for the ALU to stabilize based on the carry from lower order packages before bringing the clock low and writing into the RAM. The required clock low time (T_{CW} of Figure 5) does not have to be increased for CPU's larger than 4 bits. Page 14 shows the minimum cycles for larger machines.

IV. PACKAGE PINS

Figure 2 shows a listing of the 40 pin I/O. The microcontroller will use a standard 40 lead ceramic dip approximately 2.00 inches long and .60 inches wide. See Figure 3 for the package details. NOTE THAT V_{CC} AND GROUND ARE NOT ON THE CONVENTIONAL END PINS. This was necessary because the package current would produce too high a voltage drop in the package lead resistance out to the end pins to meet the V_{OL} requirements.

PIN CONFIGURATION

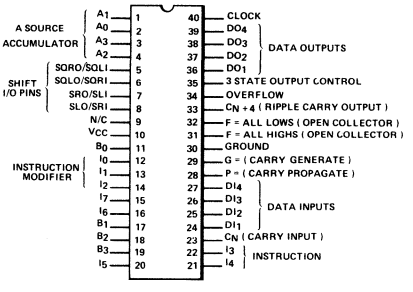
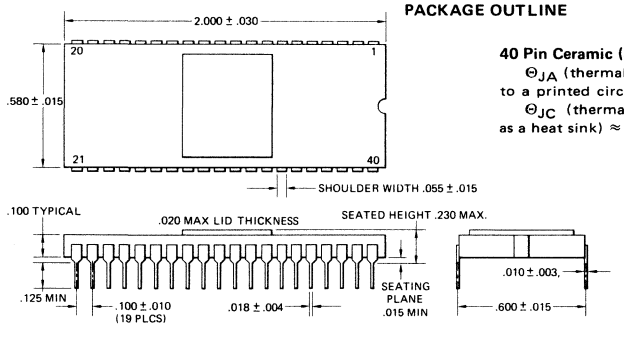


Figure 2.

PACKAGE OUTLINE



40 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) $\approx 35^{\circ}$C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) $\approx 20^{\circ}$C/watt

Figure 3.

BURN-IN CIRCUIT

The circuit in Figure 4 below puts the device in an instruction where the state of all outputs is known. Any other set of levels on the inputs may result in undefined output states and possible damage to the device under burn-in conditions. The other instructions involve the use of internal register whose initial conditions, after power-up, are undefined. The burn-in circuit shown comes closest to the usual reverse burn-in circuits of logic devices. The unit is in the force LLLL mode with the shift I/O pins disabled, the data outputs disabled, and with a single accumulator always selected.

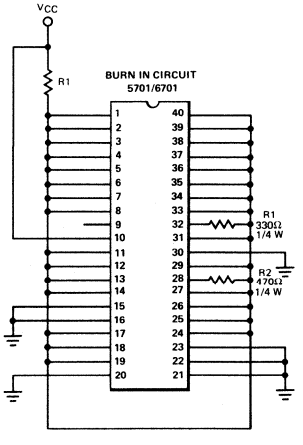


Figure 4.

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5 to 7 V
Input Voltage	−1.0 to 5.5 V
Output Current	100 mA
Input Current	−20 to 5 mA
Storage Temperature	−65 to +150°C

Stresses above or extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.

D. C. CHARACTERISTICS Unless otherwise indicated, all limits for the 6701 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5701 are guaranteed for 5 V ±10% in a free air temperature of −55 to 125°C.

PARAMETER	DEVICE PINS	CONDITIONS	5701			6701			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX	
I_F Input Load Current	Any A, B, or I	V_{CC} = Max, V_F = .45 V			-250			-250	μA
	Clock or 3 State Control	"			-250			-250	μA
	Shift I/O & Data In	"			-0.80			-0.80	mA
	C_N	"			-4.80			-4.80	mA
I_R Input Leakage Current	Any A, B, or I	V_{CC} = Max, V_R = 2.40 V			40			25	μA
	Clock or 3 State Control	"			40			25	μA
	Shift I/O	Used as an Input			100			100	μA
	Data Inputs	"			20			20	μA
	C_N	"			120			120	
I_{RB} Input Leakage Current	Any A, B, or I	V_{CC} = Max, V_{RB} = 5.50 V			1.0			1.0	mA
	Clock or 3 State Control	"			1.0			1.0	mA
	Shift I/O	"			1.0			1.0	mA
	Data Input	"			1.0			1.0	mA
	C_N	"			1.0			1.0	mA
V_{OL} Low Level Output Voltage	Data Out G, C_{N+4}, F = All High, F = All Low	V_{CC} = Min, I_{OL} = 16 mA		.35	0.50		.35	0.50	V
	P, Overflow	V_{CC} = Min, I_{OL} = 10 mA		.35	0.50		.35	0.50	V
	Shift I/O	V_{CC} = Min, I_{OL} = 6 mA Used as an Output		.35	0.50		.35	0.50	V
I_{CC} Power Supply Current	V_{CC}, Grd	All inputs ground (worst case), All Outputs Open, Shift I/O Open V_{CC} = 5.00 V and Temp = Max		215	250		215	280	mA
		All Inputs ground (worst case), All Outputs Open, Shift I/O Open V_{CC} = 5.00 V and Temp = Min		230	280		230	250	mA
V_{IL} Low Level Input Voltage	All Inputs and Shift I/O	V_{CC} = 5.00 V			0.80			0.80	V
V_{IH} High Level Input Voltage	All Inputs and Shift I/O	V_{CC} = 5.00 V	2.0			2.0			V
V_{IC} Input Clamp Voltage	All Inputs and Shift I/O	V_{CC} = Min, I_{IC} = -5.0 mA		-1.0	-1.5		-1.0	-1.5	V
I_{CEX} Output Leakage Current	All Outputs and Shift I/O	V_{CC} = Max, V_{CEX} = 2.40 V, High Stored or Disabled			100			100	μA
		V_{CC} = Max, V_{CEX} = 0.45 V Disabled			-100			-100	μA
I_{CEXB} Output Leakage Current	All Outputs and Shift I/O	V_{CC} = Max = V_{CEXB} High Stored or Disabled			1			1	mA
I_{SC} Output Short Circuit Current	DO_1, DO_2, DO_3, DO_4, G, P, OVFL,	V_{OUT} = OV, V_{CC} = 5 V Only one Output at a time should be Shorted	20	50	90	20	50	90	mA
	Shift I/O	V_{OUT} = OV, V_{CC} = 5 V Only one Output at a time should be Shorted	5	15	50	5	15	50	mA

D.C. CHARACTERISTICS (Cont'd)

PARAMETER	DEVICE PINS	CONDITIONS	5701			6701			UNITS
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX	
V_{OH} Output Voltage "High"	DO_1, DO_2, DO_3, DO_4, G, C_{N+4}	I_O = -3.2 mA, V_{CC} = Min High Stored	2.4			2.4			V
	Shift I/O, P, OVFL	I_O = - 500 μA V_{CC} = Min High Stored	2.4	3.5		2.4	3.5		V
C_I Input Capacitance	All Inputs	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz		8			8		pF
C_O Output Capacitance	All Outputs	V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz		8			8		pF

1. Typical values are measured at 5.0 V and 25°C.

A. C. CHARACTERISTICS The maximum or minimum of all possible input and output conditions is specified with outputs sinking maximum current and driving a 30pF load (15pF on Shift I/O).

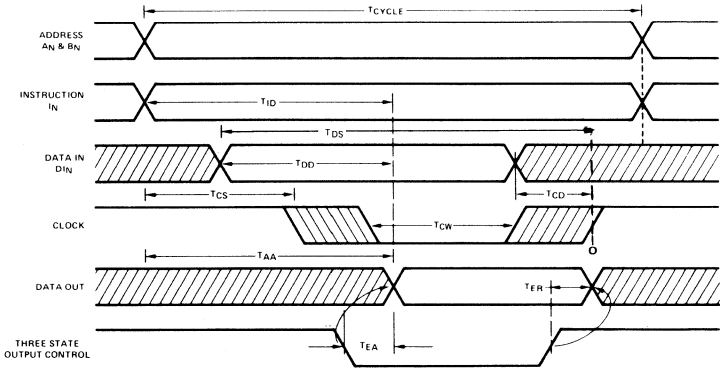
PARAMETER	SYMBOL/CONDITIONS	5 V ± 10% -55 TO 125°C 5701			5 V ± 5% 0 TO 75°C 6701			UNITS
	SEE FIGURE 5	MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
Microinstruction Clock Cycle (Time Between Instructions)	T_{CYCLE}	250	152	∞	200	152	∞	ns
Accumulator Address to Data Out Delay Thru ALU/Bypass ALU	T_{AA}	40/20	110/60	170/90	40/20	110/60	140/85	ns
Instruction to Data Out Delay	T_{ID}	40	110	175	40	110	140	ns
Clock Pulse Width	T_{CW}	80	42		60	42		ns
Clock Set-up Time	T_{CS}	115	80		80	70		ns
3 State Enable to Data Out Enable	T_{EA}	10	25	40	10	25	37	ns
3 State Disable to Output Disable	T_{ER}	5	14	25	5	14	20	ns
C_N to C_{N+4}			20	30		20	30	ns
Accumulator Address to C_{N+4}	Clock High		65	95		65	90	ns
Data In to C_{N+4}			28	42		28	40	ns
Instruction to C_{N+4}	Clock High		54	81		54	78	ns
Accumulator Address to G	Clock High		60	90		60	85	ns
Data In to G			36	54		36	50	ns
Instruction to G or P	Clock High		52	78		52	75	ns
Accumulator Address to P	Clock High		60	90		60	85	ns
Data In to P			25	40		25	37	ns
Accumulator Address to F = All Highs	Clock High		64	96		64	90	ns
Data In to F = All Highs			60	90		60	86	ns
Instruction to F = All Highs	Clock High		76	110		76	100	ns
Accumulator Address to F = All Lows	Clock High		64	96		64	90	ns
Data In to F = All Lows			40	60		40	57	ns
Instruction to F = All Lows	Clock High		60	90		60	85	ns
Accumulator Address to SLO/SRI or SRO/SLI	Clock High		95	140		95	130	ns
Data In to SLO/SRI or SRO/SLI			40	60		40	55	ns
Instruction to SLO/SRI or SRO/SLI	Clock High		75	110		75	105	ns
Instruction to SQRI/SQLO or SQRO/SQLI	Clock High		25	40		25	37	ns
Clock to Data Out Delay	A_N, B_N, C_N, D_N Stable	40	110	175	40	110	140	ns

A.C. CHARACTERISTICS (Cont'd)

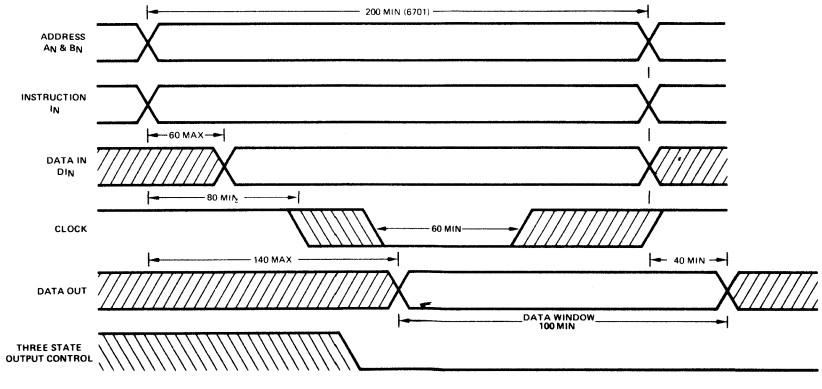
PARAMETER	SYMBOL/CONDITIONS	5 V ± 10% −55 TO 125°C			5 V ± 5% 0 TO 75°C			UNITS
	SEE FIGURE 5	5701 MIN.	5701 TYP.[1]	5701 MAX.	6701 MIN.	6701 TYP.[1]	6701 MAX.	
Data In to Data Out Delay	T_{DD} Clock High	20	60	90	20	60	80	ns
Clock to Data In Hold Time	T_{CD} Clock Low to High Transition		−20	−10		−20	−10	ns
Latest Possible Arrival of Data In Set-up Time	T_{DS} Measure Relative to End of Clock	170			140			ns
Q Register to SQLO/SQRI or SQRO/SQRI	Measured From Low to High Transition of Clock		36	54		36	50	ns
Accumulator Address to Overflow	Clock High		90	135		90	125	ns
Data In to Overflow			36	54		36	50	ns
Instruction to Overflow	Clock High		56	84		56	80	ns
C_N to Overflow			25	38		25	35	ns
C_N to Data Out	Three State Low	5	36	54	5	36	50	ns

1. Typical values are measured at 5.0 V, 25°C

TIMING DIAGRAM



SAMPLE MINIMUM CYCLE TIMING DIAGRAM FOR 6701 (4 BIT MACHINE)



LEGEND: Shaded areas indicate don't care conditions or permitted timing tolerances.

Indicates that one pulse edge causes the other and that the two edges track.

FIGURE 5

INSTRUCTIONS LOCATED IN THE ON CHIP ROMS

SYMBOL DEFINITIONS

A_I = Any of the 16 four bit registers in the multiport RAM (I = O to 15)
B_J = " " (J = 0 to 15)
$A_I + B_J$ = A_I plus B_J (arithmetic addition)
$A_I \forall B_J$ = A_I exclusive OR'ed with B_J
$A_I \vee B_J$ = A_I or B_J (logic inclusive or)
$A_I \wedge B_J$ = A_I and B_J (logic and)
$\overline{A_I}$ = The complement of A_I
$A_I \longrightarrow Q$ = Transfer A_I to Q, A_I saved, Old Q is lost
$A_I \longrightarrow OUT$ = Transfer A_I to the output pins, A_I is saved

$\overrightarrow{A_I}$ = A_I shifted right one bit

$\overleftarrow{A_I}$ = A_I shifted left one bit
$B_J - A_I$ = B_J minus $A_I = B_J + \overline{A_I} + C_N = B_J$ + 2's compl. of A_I

POSITIVE (ACTIVE HIGH) VS. NEGATIVE (ACTIVE LOW) LOGIC

The Microcontroller will work with either positive or negative logic. Positive logic defines a TTL High Level (≈ 3V) to be a "I" and a Low TTL Level (≈ GRD) to be a "O". Negative logic defines a TTL High to be A "O" and a TTL Low to be a "I". Consider a a classical "AND" function in TTL Logic

OUTPUT	INPUTS	
	B	A
L	L	L
L	L	H
L	H	L
H	H	H

in positive logic this becomes

OUTPUT	INPUTS	
	B	A
O	O	O
O	O	I
O	I	O
I	I	I

In negative logic the "AND" becomes an "OR" function since:

OUTPUT	INPUTS	
	B	A
I	I	I
I	I	O
I	O	I
O	O	O

Thus an "AND" in positive logic is an "OR" in negative logic. Similar reasoning yields the following transformations.

POSITIVE LOGIC	NEGATIVE LOGIC
AND	OR
OR	AND
EXCLUSIVE OR	EXCLUSIVE NOR
EXCLUSIVE NOR	EXCLUSIVE OR
TRANSFER	DECREMENT
DECREMENT	TRANSFER
INCREMENT	TRANSFER
TRANSFER	INCREMENT

CARRY IN (C_N)

The carry in pin is high when a carry is desired in positive logic, and a low when a carry is desired in negative logic.

TWO ROMS

All of the instructions in the 32 x 9 ROM can be modified in 8 different ways by the 8 x 8 ROM. Any instruction for example can be shifted left or right with the data out pins showing A, B, or F and the shifted result stored in the RAM or Q Register or both. If the clock is gated OFF by external logic it will be impossible to load the RAM or Q Register, and the controlled use of C_N in many instructions further raises the instruction count.

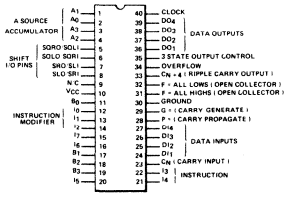
INSTRUCTIONS IN THE 32 x 9 ROM – POSITIVE LOGIC (1 = H ≈ 3 V) INTERPRETATION

ROM WORD							ALU Instruction (See Pg. 8 for Symbology)	ALU OUTPUT		TYPICAL USES	
I_7	I_6	I_5	I_4	I_3	Decimal	Octal		No Carry In (C_N = L)	With Carry In (C_N = H)		
L	L	L	L	L	0	00	LLLL + HHHH + C_N	Force 1111	Force 0000	Initialization (Force 1's or 0's)	
L	L	L	L	H	1	01	AND A_I & B_j	$A_I \wedge B_j$	$A_I \wedge B_j$	AND	A_I & B_j
L	L	L	H	L	2	02	AND D_1 & B_j	$D_I \wedge B_j$	$D_I \wedge B_j$	"	D_I & B_j
L	L	L	H	H	3	03	OR A_I & B_j	$A_I \vee B_j$	$A_I \vee B_j$	OR	A_I & B_j
L	L	H	L	L	4	04	OR D_I & B_j	$D_I \vee B_j$	$D_I \vee B_j$	"	D_I & B_j
L	L	H	L	H	5	05	Exclusive OR A_I & B_j	$A_I \veebar B_j$	$A_I \veebar B_j$	Exclusive Or	A_I & B_j
L	L	H	H	L	6	06	Exclusive OR D_I & B_j	$D_I \veebar B_j$	$D_I \veebar B_j$	"	D_I & B_j
L	L	H	H	H	7	07	$\overline{A_I}$ + HHHH + C_N	$\overline{A_I}$ + 1111	$\overline{A_I}$	Invert	A_I
L	H	L	L	L	8	10	$\overline{D_I}$ + HHHH + C_N	$\overline{D_I}$ + 1111	$\overline{D_I}$	"	D_I
L	H	L	L	H	9	11	$\overline{B_j}$ + HHHH + C_N	$\overline{B_j}$ + 1111	$\overline{B_j}$	"	B_j
L	H	L	H	L	10	12	$\overline{Q}$ + HHHH + C_N	$\overline{Q}$ + 1111	$\overline{Q}$	"	Q
L	H	L	H	H	11	13	$\overline{A_I}$ + LLLL + C_N	$\overline{A_I}$	$\overline{A_I}$ + 0001	2's Complement Of	A_I
L	H	H	L	L	12	14	$\overline{D_I}$ + LLLL + C_N	$\overline{D_I}$	$\overline{D_I}$ + 0001	"	D_I
L	H	H	L	H	13	15	$\overline{B_j}$ + LLLL + C_N	$\overline{B_j}$	$\overline{B_j}$ + 0001	"	B_j
L	H	H	H	L	14	16	$\overline{Q}$ + LLLL + C_N	$\overline{Q}$	$\overline{Q}$ + 0001	"	Q
L	H	H	H	H	15	17	A_I + LLLL + C_N	A_I	A_I + 0001	Transfer Or Increment	A_I
H	L	L	L	L	16	20	D_I + LLLL + C_N	D_I	D_I + 0001	"	D_I
H	L	L	L	H	17	21	B_j + LLLL + C_N	B_j	B_j + 0001	"	B_j
H	L	L	H	L	18	22	Q + LLLL + C_N	Q	Q + 0001	"	Q
H	L	L	H	H	19	23	A_I + HHHH + C_N	A_I + 1111	A_I	Decrement Or Transfer	A_I
H	L	H	L	L	20	24	D_I + HHHH + C_N	D_I + 1111	D_I	"	D_I
H	L	H	L	H	21	25	B_j + HHHH + C_N	B_j + 1111	B_j	"	B_j
H	L	H	H	L	22	26	Q + HHHH + C_N	Q + 1111	Q	"	Q
H	L	H	H	H	23	27	A_I + B_j + C_N	A_I + B_j	A_I + B_j + 0001	Add	A_I & B_j
H	H	L	L	L	24	30	D_I + B_j + C_N	D_I + B_j	D_I + B_j + 0001	"	D_I & B_j
H	H	L	L	H	25	31	A_I + Q + C_N	A_I + Q	A_I + Q + 0001	"	A_I & Q
H	H	L	H	L	26	32	D_I + Q + C_N	D_I + Q	D_I + Q + 0001	"	D_I & Q
H	H	L	H	H	27	33	A_I + $\overline{B_j}$ + C_N	A_I - B_j - 0001	A_I - B_j	Subtract	A_I & B_j
H	H	H	L	L	28	34	B_j + $\overline{A_I}$ + C_N	B_j - A_I - 0001	B_j - A_I	"	B_j & A_I
H	H	H	L	H	29	35	D_I + $\overline{B_j}$ + C_N	D_I - B_j - 0001	D_I - B_j	"	D_I & B_j
H	H	H	H	L	30	36	B_j + $\overline{D_I}$ + C_N	B_j - D_I - 0001	B_j - D_I	"	B_j & D_I
H	H	H	H	H	31	37	D_I + $\overline{Q}$ + C_N	D_I - Q - 0001	D_I - Q	"	D_I & Q

INSTRUCTION MODIFIERS IN THE 8 x 8 ROM – POSITIVE LOGIC (1 = H ≈ 3 V) INTERPRETATION

Rom Word			Rom Word	Load Control		Shift Control		Data Out Control			
I_2	I_1	I_0	Decimal	Load Ram B_j	Load Q	Shift Left	Shift Right	Don't Shift	A Latch	B Latch	ALU Output F
L	L	L	0	X				X			X
L	L	H	1	X				X	X		
L	H	L	2	X				X		X	
L	H	H	3	X		X					X
H	L	L	4	X			X				X
H	L	H	5	X	X	X					X
H	H	L	6	X	X		X				X
H	H	H	7		X			X			X

PIN CONFIGURATION



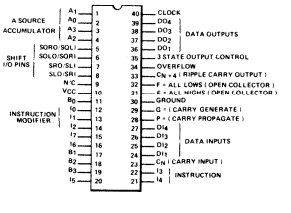
INSTRUCTIONS IN THE 32 x 9 ROM – NEGATIVE LOGIC (1 = L ≈ 0 V) INTERPRETATION

ROM WORD							ALU Instruction (See Pg. 8 for Symbology)	ALU OUTPUT		TYPICAL USES	
I_7	I_6	I_5	I_4	I_3	Decimal	Octal		No Carry In (C_N = H)	With Carry In (C_N = L)		
L	L	L	L	L	31	37	LLLL + HHHH + C_N	Force 1111	Force 0000	Initialization (Force 1's or 0's)	
L	L	L	L	H	30	36	OR A_I & B_j	A_I V B_j	A_I V B_j	OR	A_I & B_j
L	L	L	H	L	29	35	OR D_I & B_j	D_I V B_j	D_I V B_j	"	D_I & B_j
L	L	L	H	H	28	34	AND A_I & B_j	A_I Λ B_j	A_I Λ B_j	AND	A_I & B_j
L	L	H	L	L	27	33	AND D_I & B_j	D_I Λ B_j	D_I Λ B_j	"	D_I & B_j
L	L	H	L	H	26	32	Exclusive OR A_I & B_j	A_I ⊻ B_j	A_I ⊻ B_j	Exclusive Nor	A_I & B_j
L	L	H	H	L	25	31	Exclusive OR D_I & B_j	D_I ⊻ B_j	D_I ⊻ B_j	"	D_I & B_j
L	L	H	H	H	24	30	$\overline{A_I}$ + HHHH + C_N	$\overline{A_I}$	$\overline{A_I}$ + 0001	2's Complement Of	A_I
L	H	L	L	L	23	27	$\overline{D_I}$ + HHHH + C_N	$\overline{D_I}$	$\overline{D_I}$ + 0001	"	D_I
L	H	L	L	H	22	26	$\overline{B_j}$ + HHHH + C_N	$\overline{B_j}$	$\overline{B_j}$ + 0001	"	B_j
L	H	L	H	L	21	25	$\overline{Q}$ + HHHH + C_N	$\overline{Q}$	$\overline{Q}$ + 0001	"	Q
L	H	L	H	H	20	24	$\overline{A_I}$ + LLLL + C_N	$\overline{A_I}$ + 1111	$\overline{A_I}$	Invert	A_I
L	H	H	L	L	19	23	$\overline{D_I}$ + LLLL + C_N	$\overline{D_I}$ + 1111	$\overline{D_I}$	"	D_I
L	H	H	L	H	18	22	$\overline{B_j}$ + LLLL + C_N	$\overline{B_j}$ + 1111	$\overline{B_j}$	"	B_j
L	H	H	H	L	17	21	$\overline{Q}$ + LLLL + C_N	$\overline{Q}$ + 1111	$\overline{Q}$	"	Q
L	H	H	H	H	16	20	A_I + LLLL + C_N	A_I + 1111	A_I	Decrement Or Transfer	A_I
H	L	L	L	L	15	17	D_I + LLLL + C_N	D_I + 1111	D_I	"	D_I
H	L	L	L	H	14	16	B_j + LLLL + C_N	B_j + 1111	B_j	"	B_j
H	L	L	H	L	13	15	Q + LLLL + C_N	Q + 1111	Q	"	Q
H	L	L	H	H	12	14	A_I + HHHH + C_N	A_I	A_I + 0001	Transfer Or Increment	A_I
H	L	H	L	L	11	13	D_I + HHHH + C_N	D_I	D_I + 0001	"	D_I
H	L	H	L	H	10	12	B_j + HHHH + C_N	B_j	B_j + 0001	"	B_j
H	L	H	H	L	9	11	Q + HHHH + C_N	Q	Q + 0001	"	Q
H	L	H	H	H	8	10	A_I + B_j + C_N	A_I + B_j	A_I + B_j + 0001	Add	A_I & B_j
H	H	L	L	L	7	07	D_I + B_j + C_N	D_I + B_j	D_I + B_j + 0001	"	D_I & B_j
H	H	L	L	H	6	06	A_I + Q + C_N	A_I + Q	A_I + Q + 0001	"	A_I & Q
H	H	L	H	L	5	05	D_I + Q + C_N	D_I + Q	D_I + Q + 0001	"	D_I & Q
H	H	L	H	H	4	04	A_I + $\overline{B_j}$ + C_N	A_I - B_j - 0001	A_I - B_j	Subtract	A_I & B_j
H	H	H	L	L	3	03	B_j + $\overline{A_I}$ + C_N	B_j - A_I - 0001	B_j - A_I	"	B_j & A_I
H	H	H	L	H	2	02	D_I + $\overline{B_j}$ + C_N	D_I - B_j - 0001	D_I - B_j	"	D_I & B_j
H	H	H	H	L	1	01	B_j + $\overline{D_I}$ + C_N	B_j - D_I - 0001	B_j - D_I	"	B_j & D_I
H	H	H	H	H	0	00	D_I + $\overline{Q}$ + C_N	D_I - Q - 0001	D_I - Q	"	D_I & Q

INSTRUCTION MODIFIERS IN THE 8 x 8 ROM – NEGATIVE LOGIC (1 = L ≈ 0 V) INTERPRETATION

Rom Word			Rom Word	Load Control		Shift Control			Data Out Control		
I_2	I_1	I_0	Decimal	Load Ram B_j	Load Q	Shift Left	Shift Right	Don't Shift	A Latch	B Latch	ALU Output F
L	L	L	7	X				X			X
L	L	H	6	X				X	X		
L	H	L	5	X				X		X	
L	H	H	4	X		X					X
H	L	L	3	X			X				X
H	L	H	2	X	X	X					X
H	H	L	1	X	X		X				X
H	H	H	0		X			X			X

PIN CONFIGURATION



APPLICATION TRICKS WITH SOME INSTRUCTIONS

1) $A_I \wedge B_J$ or $A_I \vee B_J$ can be used as a no operation if $A_I = B_J$ and only the RAM is loaded since we are loading a register with itself.

2) $A_I \forall B_J$ can be used to load LLLL if $A_I = B_J$ regardless of the state of C_N.

3) $A_I + B_J + C_N$ gives $A_I + A_I + C_N$ if $A_I = B_J$, forming twice "A" or twice (A + I). IF $A_I + B_J + C_N$ is shifted left with $A_I = B_J$, we get a double left shift since adding a number to itself is a multiply by 2 which in binary is a shift left.

4) Q can be shifted and stored back in Q during any instruction involving HLH or HHL on I_2, I_1, I_0 permitting simultaneous RAM and Q shifting. Operations involving 3 registers (A, B, and Q) are also possible since we can perform A + B ⟵ Q.

5) B_J + LLLL + $C_N \longrightarrow B_J$
B_J + HHHH + $C_N \longrightarrow B_J$
can be used as a NO OP if there is no carry

6) B_J + LLLL + $C_N \longrightarrow B_J$, $A_I \longrightarrow$ OUT
B_J + HHHH + $C_N \longrightarrow B_J$, $A_I \longrightarrow$ OUT

Permits use of one of the B_J for a program counter (P.C) while looking at one of the A_I which might be an accumulator on the output pins. If there is a carry,
B_O + 0001 ⟶ B_O (Increment P.C)
A_I ⟶ OUT (Old P.C ⟶ OUT)
Might be used to increment the program counter while having the old value of the program counter addressing memory (via the data out pins) in one microcontroller cycle.

CARRY GENERATE (G) AND CARRY PROPAGATE (P)

A) THEORY

The G and P pins of the microcontroller are designed to be used with the TTL 54182/74182 look-ahead carry generator. The look-ahead techniques predict whether or not there will be a carry generated from the microcontroller and whether the input carry (C_N) will be propagated through the microcontroller, based on the input operands rather than waiting for the carry to ripple through each internal stage of the microcontroller. The add times of larger word length machines are significantly faster with these techniques.

B) ACTIVE HIGH AND ACTIVE LOW LOGIC

G and P are sometimes called X and Y in active HIGH (Positive) logic terminology since the generate and propagate terminology are pertinent only to active LOW (Negative) logic. The microcontroller and look-ahead carry generator will produce the correct results in both active HIGH and active LOW logic. Figure 6 shows how to hook-up the look-ahead carry generator (74182 or 74S182).

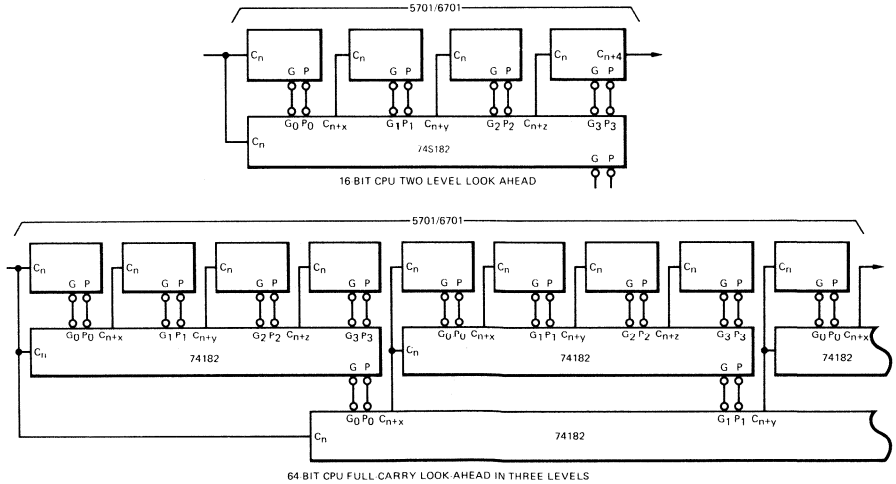


FIGURE 6

C) LOGIC EQUATION

In logic symbology where J is a logic "AND" and + is a logic "OR" and where the subscript L means a low TTL logic level; P can be expressed as follows:

$$Y = P_L = (A'3_H + B'3_H) \cdot (A'2_H + B'2_H) \cdot (A'1_H + B'1_H) \cdot (A'0_H + B'0_H)$$

This equation is interpreted to mean that propagate is a low level if $A'3$ or $B'3$ is high and $A'2$ or $B'2$ is high, and $A'1$ or $B'1$ is high, and $A'0$ or $B'0$ is high. $A'3$, $A'2$, $A'1$, $A'0$, and $B'3$, $B'2$, $B'1$, $B'0$ refer to the four bit number applied at the input A' and B' of the microcontroller ALU.

In the same symbology:

$$X = G_L = (A'3_H \cdot B'3_H) + (A'3_H + B'3_H) \cdot (A'2_H \cdot B'2_H) + (A'3_H + B'3_H) \cdot (A'2_H + B'2_H) \cdot$$

$$(A'1_H \cdot B'1_H) + (A'3_H + B'3_H) \cdot (A'2_H + B'2_H) \cdot (A'1_H + B'1_H) \cdot (A'0_H \cdot B'0_H)$$

RIPPLE CARRY (C_{N+4})

In systems not requiring the speed of look-ahead addition the 74S182 look-ahead carry generator can be eliminated and the ripple carry C_{N+4} can be used instead. Simply tie the ripple carry output C_{N+4} of the least significant microcontroller package to the carry input C_N of the more significant microcontroller package. Figure 7 shows some examples of ripple carry and combined ripple and look-ahead carry.

The ripple carry output will be a TTL high level when a carry out occurs in the active HIGH (Positive) logic convention. The ripple carry output will be a TTL low level when a carry out occurs in the active LOW (Negative) logic convention.

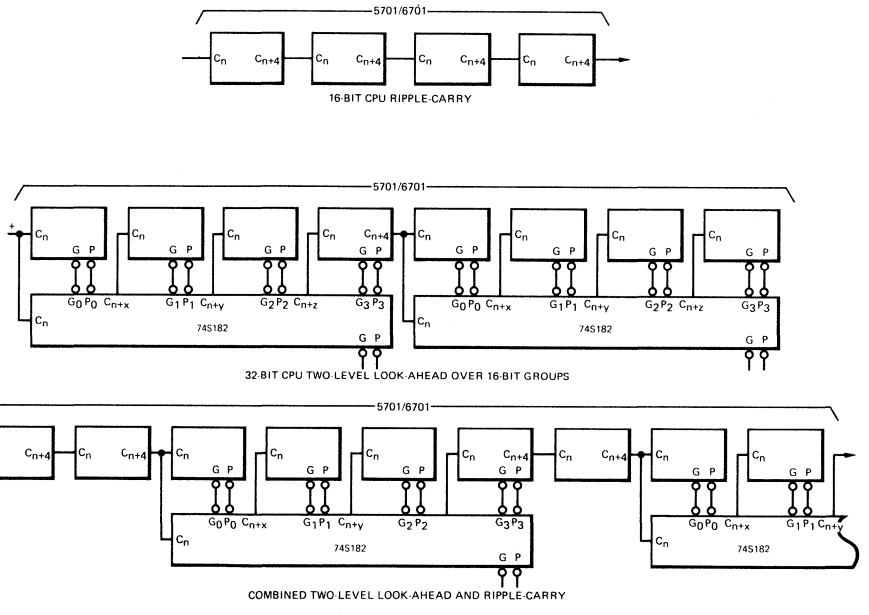


FIGURE 7

WORST CASE MINIMUM CYCLE TIMES OVER THE V_{CC} AND TEMPERATURE RANGE FOR CPU'S LARGER THAN 4 BITS

CPU Word Length (# Bits)	Minimum Cycle With Ripple Carry (ns)	6701 Minimum Cycle* With Look Ahead		Minimum Cycle With Ripple Carry (ns)	5701 Minimum Cycle* With Look Ahead	
		#Look Ahead 74S182's	Cycle Time (ns)		#Look Ahead 74S182's	Cycle Time (ns)
4	200			250		
8	200			250		
		1	205		1	250
12	230			259		
		1	205		1	250
16	260			289		
		1	205		1	250
24	320			349		
		1	245		1	284
		2	215		2	254
32	380			409		
		1	300		1	334
		2	245		2	284
		3	215		3	254
48	500			529		
		1	420		1	454
		2	340		2	379
		3	285		3	329
		4	215		4	254
64	620			649		
		1	540		1	574
		2	460		2	499
		3	380		3	424
		4	325		4	374
		5	215		5	254

*The minimum look-ahead cycle times assume a 74S182 with a delay of 10ns maximum for 5 V ± 5%, 0° to 75°C or a 54S182 with a delay of 15ns maximum for 5 V ±10%, –55° to 125°C.

NOTE

The worst case instruction from a cycle time consideration is an add shift, and store instruction in one cycle. The cycle times above are based on this instruction.

THEORY

The delay from A_I or B_J to data output can be assumed to equal the delay from A_I or B_J to the data inputs of the on chip RAM. The increase in the delay from A_I or B_J to data out due to waiting for the carry in, over the case where the carry in is present early is a direct cycle time adder.

SAMPLE CALCULATION OF THE CYCLE FOR A 32 BIT MACHINE AND THE REQUIRED CLOCK TIMING

Calculate the minimum cycle time of the 6701 in a 32 bit configuration. Two 74S182's will be used to look ahead over the two 16 bit section with ripple carry between the two 16 bit sections (see the center drawing of Figure 7 page 13).

From page 7 the accumulator address to G or P delay is 85ns it will then take another 10ns in the 74S182 to generate C_{N+X}, C_{N+Y}, and C_{N+Z} the C_N to output delay (50ns) is faster than the accumulator to data out delay (85ns) in the least significant package hence the 85ns path will limit the speed of the 74S182.

HARDWARE MULTIPLY AND DIVIDE

I. GENERAL DISCUSSION

The microcontroller's capability of adding and shifting or subtracting and shifting within one microinstruction cycle, and having the accumulator extension register Q on chip permits fast microprogrammed multiply and divide. Less than 20 cycles are required for a 16 bit multiply or divide.

Figure 8 shows how to hook up the microcontroller for a 16 bit multiply/divide. The least significant bit of the RAM shifter is shifted into the most significant bit of Q.

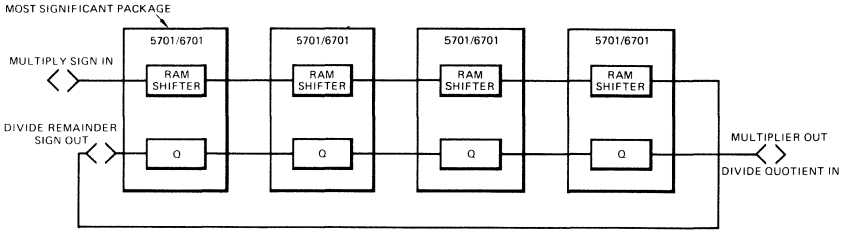


FIGURE 8

II. HARDWARE MULTIPLY – EXAMPLE FOR A 16 BY 16 MULTIPLY

A. INITIAL CONDITIONS

Put the multiplier in Q, multiplicand on the RAM A output, and clear the RAM B output to zero.

B. FINAL CONDITIONS

The most significant 16 bit half of the 32 bit product will be in RAM B and the least significant 16 bit half in Q. The multiplicand in A is undisturbed.

C. THEORY

A 16 by 16 multiply in the microcontroller requires 16 reduction steps. Each reduction step consists of an add (A+B), if the least significant bit or the multiplier emerging from Q is a one, or a transfer (0+B) if the least significant bit of Q is a zero, and then a right shift of the result into B and Q.

D. TWO'S COMPLEMENT

Two's complement multiplication requires sign bit manipulation and an additional correction cycle for negative multipliers. The sign inserted into the most significant bit of B during the reduction cycles is the OR of the most significant bit of B and the most significant bit of the ALU output. After 16 reduction cycles, an additional correction cycle is required if the multipliers was negative. The correction cycle consists of subtracting the multiplicand from the product without shifting.

III. HARDWARE DIVIDE

Example for a 16 bit divisor and 32 bit dividend giving a 16 bit quotient and 16 bit remainder.

A. INITIALIZATION

Put the divisor on the RAM A output, and the dividend's most significant half on the RAM B output and the least significant half in Q.

B. FINAL CONDITION

The 16 bit quotient is on the RAM B output and the 16 bit remainder is in Q. The divisor is in the RAM A output undisturbed.

C. THEORY

A non-restoring two's complement division requires 16 reduction steps for negative quotients. In non-restoring division, the divisor is successively subtracted from the dividend and the result shifted left until the remainder changes sign. At this point the divisor has been subtracted one too many times and is added back until the original sign is restored.

Negative quotients are generated in one's complement notation (the one's complement of a number is its inverse). The two correction cycles provide a remainder correction if required so that the remainder sign is the same as the original dividend and quotient correction from one's complement to two's complement form for negative quotients.

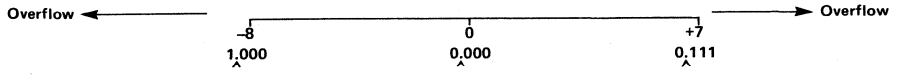
Each of the 16 reduction cycles consists of a subtract (B–A) or an add (A+B) operation plus a left shift of the result. The most significant bit of Q propagates into the least significant bit of B and the quotient bit is shifted into the least significant vacated position of Q. The case of zero remainder will not require quotient correction but may require sign correction of the remainder.

With C_{N+Z} generated at 95ns, the C_N to C_{N+4} delay (30ns) of package 4 (bits 12 to 16) is in the critical path. Generation of C_N to package 5 will arrive at 125ns. C_{N+Z} into package 8 will arrive at 135ns. The C_N to output delay of package 8 (50ns) will now let the data out of the package reflect the correct outputs by 185ns. Since the F bus of the 6701 ALU has gone thru the output buffers by 185ns, we can assume that by 185ns the F bus has been shifted and is stable at the data inputs of the 6701's RAM. We must now bring the clock low for 60ns from time 185 to 245ns to write the shifted result in the RAM. The complete add, shift, and store cycle is hence 245ns. The data outputs of package 8 (bits 28 to 32) will reflect the results of the addition in 185ns. Note that the chart above reflects a 245ns cycle time for two 74S182's and a 32 bit CPU.

OVERFLOW

THEORY

When the result of a binary addition or subtraction requires more bits than the arithmetic unit can accommodate overflow can occur. For example, consider a 4-bit system (3 bits + sign) where the most significant bit is defined on a zero for positive numbers and a one for negative numbers. This system has a maximum value of 7 and a minimum value of –8 as indicated on the line graph below:



If we list all the addition and subtraction conditions which will give an answer not in the number system (beyond the ends of the line graph above), four conditions result in overflow and are listed below with examples:

OVERFLOW CONDITIONS

1. **ADD TWO LARGE POSITIVE NUMBERS**
   7 plus 7 = 14, which is larger than our largest number (+7) on the line graph, therefore, overflow occurs
   2 plus 1 = 3, which is smaller than +7, therefore, no overflow

2. **ADD TWO LARGE NEGATIVE NUMBERS**
   –7 plus –7 = –14, which is beyond the end of the line graph, therefore, overflow occurs.
   –2 plus –1 = –3, no overflow since –3 is within the bounds of the number system

3. **SUBTRACT A LARGE NEGATIVE NUMBER FROM A LARGE POSITIVE NUMBER**
   –7 minus +7 = –14, overflow occurs
   –2 minus +1 = –3, no overflow

4. **SUBTRACT A LARGE POSITIVE NUMBER FROM A LARGE NEGATIVE NUMBER**
   +7 minus –7 = +14, overflow occurs
   +2 minus –1 = +1, no overflow

OVERFLOW PIN ON THE MICROCONTROLLER

A conventional binary number system has the most significant bit defined as the sign bit (0 is a positive number, 1 is a negative number by definition) and negative numbers are represented in a 2's complement form (the 2's complement of a number can be formed by inverting the number and adding one, for example, 0101 = +5, –5 = 1010 plus 1 or 1011.

The four overflow conditions shown above can be detected by exclusive ORing the carry-in and carry-out of the sign bit. If the carry's disagree, overflow has occurred. The overflow output will only be meaningful on the most significant microcontroller package in systems larger than four bits. Since the overflow is implemented with an exclusive nor gate the microcontroller will also give overflow outputs during logic as well as arithmetic operations requiring that external logic decide when the overflow output is meaningful. The overflow pin will be low when overflow occurs.

SIGN EXTENSION

A common operation in computers is the calculation of an effective address. In a 16 bit computer, for example, we may have program counter relative addressing, where the addition of an 8 bit displacement to a 16 bit program counter is the effective memory address. This 8 bit displacement is a signed displacement with a value between +127 and −128.

In using the 5701/6701 to calculate on effective address, the displacement will be brought into the unit with the data in pins, and added to the program counter which is stored in one of the internal registers. The problem arises when adding on 8 bit number to a 16 bit number in that the upper 8 bits of the displacement must be ignored and the sign of the 8 bit displacement (a 0 in bit 8 is a plus and a 1 is a minus) must be extended into bits 9 thru 16 to make a signed 8 bit number into a proper signed 16 bit number. For example the 8 bit displacement 01111111 is +127 and must be translated into the 16 bit number 0000000001111111 before adding it to the 16 bit program counter.

Several techniques can be used to extend the sign. Figure 9 shows dual 4 bit selects (74157) which are used to duplicate the sign bit (bit 8) into the upper 8 bits. The 74157's either let the normal upper 8 bits of the data in bus or the sign bit extended into the upper 8 bits of the 5701/6701's data in depending on whether the multipler's select line is high or low. The instruction lines of the 5701/6701's required for 16 bits can be wired to common pins in the 4 packages with this approach. Bit 8 can be buffered if the loading of the 74157 would be a problem.

Another technique is shown in Figure 10, and is applicable only when ripple carry is employed. It requires that the two low order packages execute a data in plus register operation and that the 2 high order package execute a LLLL plus HHHH plus C_N instruction. If C_N is low and the 7451 is in the sign extend mode, then highs will be forced into the upper two packages. If C_N is a high and the 7451 is in the extend sign mode, then lows will be forced into the high order packages. When the sign is not to be extended the 7451 will pass the C_{N+4} ripple carry into C_N. This method requires that the lower two 5701/6701's execute a different instruction than the upper two 5701/6701's. This particular case will require changing the state of two of the 8 instruction lines which go into the upper two 5701/6701's, namely the I_6 and I_7 lines. Note that in the instruction on page 10, these instruction were purposely mapped so that few I_N lines must be changed to go from LLLL + HHHH + C_N to $D_I + B_J + C_N$.

A third alternative is to microprogram the sign extension with off chip ROMs by masking or forcing the upper 8 bits.

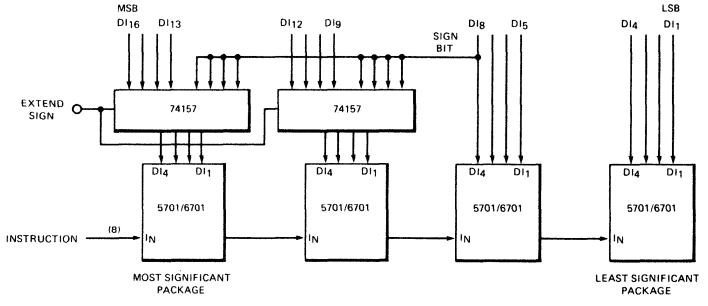


FIGURE 9

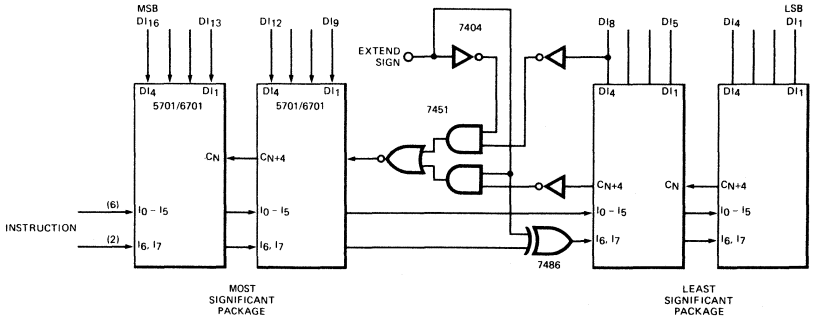


FIGURE 10

MICROPROGRAMMED EMULATION

Figure 11 shows a 16 bit microprogrammed CPU built from 4 microcontrollers, a few ROMs and some TTL. This CPU performs about the same function as most 16 bit minicomputer's CPU which take 110 to 225 TTL MSI packages, and require one or two 15" x 15" printed circuit boards. The CPU of Figure 11 requires 18 packages and will fit on 5" x 7" board.

HOW IT WORKS

The four microcontrollers form the data flow section of the CPU. The zero detect (F = LLLL and F = HHHH) pins of the 6701 are open collector and are tied together to detect zero on the 16 bit CPU. The 3 state output control and clock lines as well as the instruction and accumulator addresses are tied to the same pins in all 4 6701's. The data flow section has 16 bits of data in and 16 bits of data out on 2 independent busses.

A programmable ROM is used to detect the various conditions which cause branching (i.e., overflow, negative, zero, etc.) and this information is fed into the sequence control section of the CPU to alter the next state when necessary.

The instruction register of the computer is the address input to the target address ROM. It points to the starting address of a group of addresses in the 1K x 24 ROM which handles the function indicated by the operation code (op-code). The instruction register is assumed to have an instruction format comprised of an 8 bit op-code, a 4 bit operand #1 select and a four bit operand #2 select like the RR format of the IBM 360.

For example, an instruction register containing might mean add file 3 to file 5 and store the result in file 5. The add assembly language instruction might point to decimal address 25 (0011001) in the target address ROM which would then output the starting address of the sequence in the emulation ROM for performing addition. A typical assembly language instruction might take 4 to 10 words in the 1K x 24 ROM.

Op Code	File	File
00011001	0101	0011

The microinstruction cycle time of the 16 bit CPU shown will be in the 350ns range. Since the microcontroller executes several operations in one cycle this CPU will execute instructions faster than most 16 bit minicomputers if semiconductor RAM is used.

The sequence of operations is programmed into the 1K x 24 for each instruction. A typical sequence for a memory reference instruction is shown below:

1. Calculate the effective address and latch it into the memory address register.
2. Fetch the contents of the memory location and latch it into the instruction register. If the memory has a 160ns or less access time, this step will not cost a microcontroller cycle.
3. Execute the instruction which is now present in the instruction register. Each clock pulse will output the required instruction to the microcontroller. When the sequence is ended the 1K x 24 ROM will disable the dual 10 bit select multiplexer gate which has been forming its next address and allow the next op-code in via the starting address ROM.
4. Increment the program counter and fetch the next instruction. A typical memory reference instruction will take 3 microcycles which includes most addressing modes, except indirect addressing. A 160ns access time, or less access time memory is required for emulation in 3 microcycles.

EMULATION

The advantage of the microprogrammed CPU described above is that it readily permits a machine designed with a new technology to be software compatible with an existing machine. The hardware technique is called emulation. Emulation protects the manufacturer's and customer's large investment in software.

The CPU configuration shown in Figure 11 can be used in many design applications where microprogrammed control might be thought of as too complicated, now that the package count has been reduced by the LSI microcontroller.

APPLICATION INFORMATION (Cont'd)

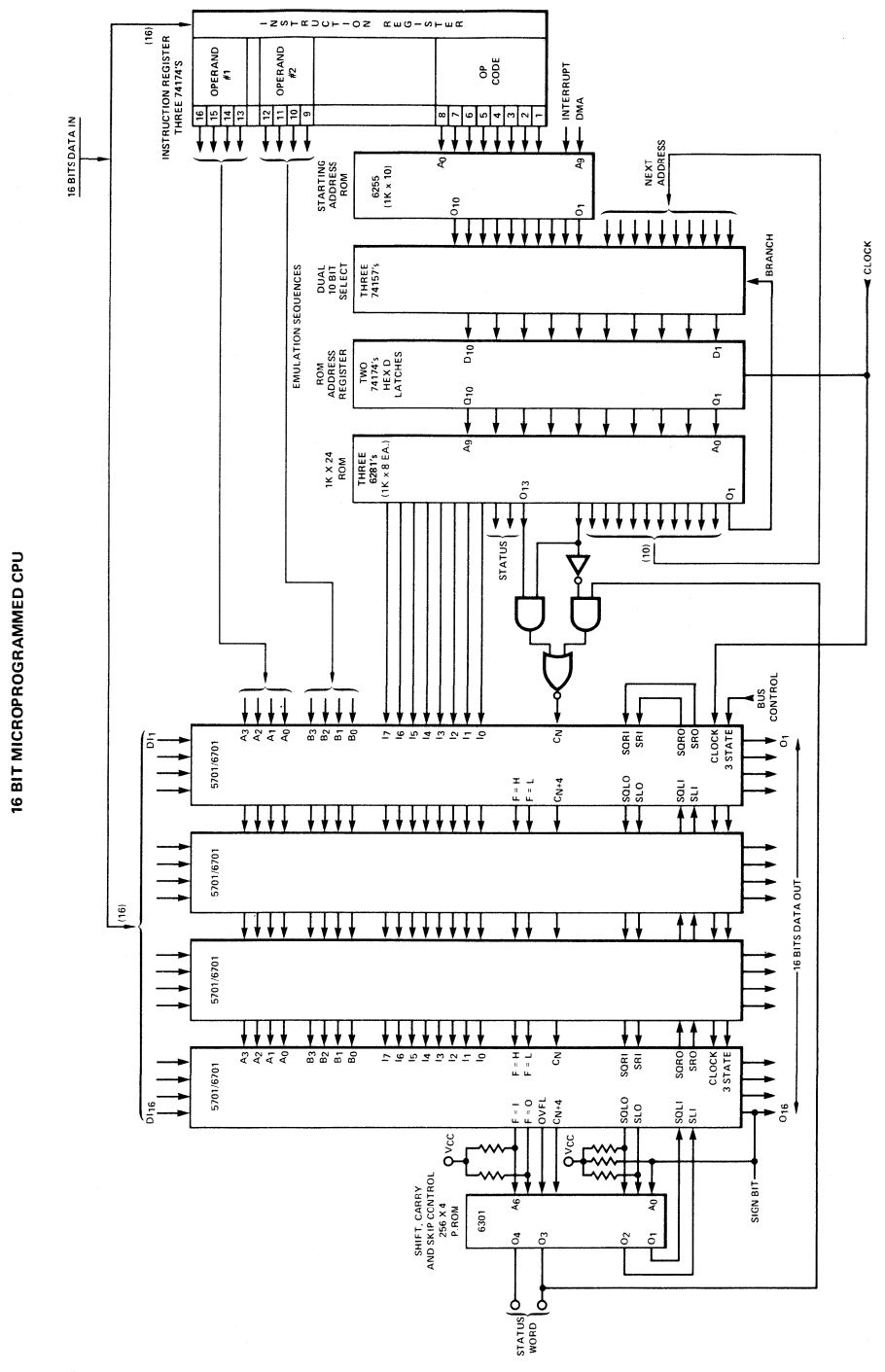


FIGURE 11

64 WORD × 4-BIT (64×4) FIRST-IN, FIRST-OUT (FIFO) SERIAL MEMORY

5741/6741

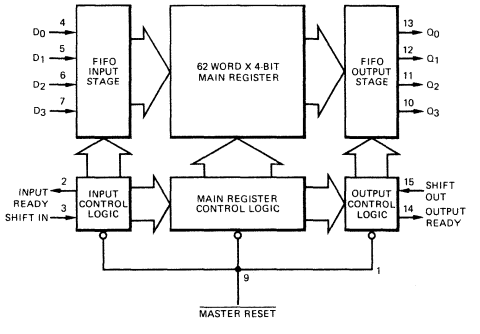
Monolithic Memories
INCORPORATED

PRODUCT FEATURES

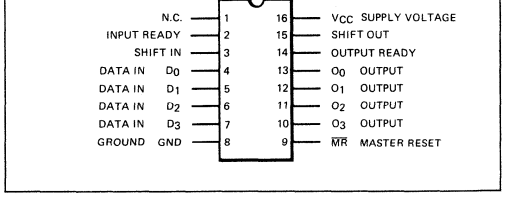
- 10 MHz Shift In, Shift Out, Rates
- Advanced Schottky Bipolar Processing
- TTL Inputs and Outputs
- Readily Expandable in Word and Bit Dimensions
- Asynchronous or Synchronous Operation
- Pin Compatible with Fairchild's F3341 MOS FIFO and Ten Times as Fast

	MILITARY	COMMERCIAL
6741		X
5741	X	

LOGIC DIAGRAM



PIN CONFIGURATION

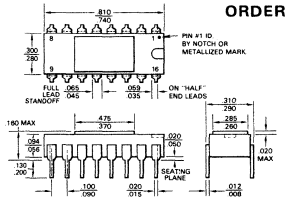


PACKAGE OUTLINE

16 PIN CERAMIC (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/watt

Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt



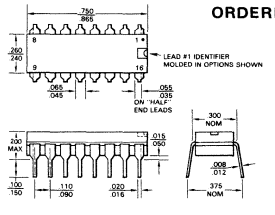
ORDERING INFORMATION

USE THE SUFFIX D
EXAMPLE 6741D

16 PIN PLASTIC

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 86°C/watt

Θ_{JC} (thermal resistance from junction to junction to case with freon as a heat sink) ≈ 36°C/watt



ORDERING INFORMATION

USE THE SUFFIX N
EXAMPLE; 6741N

Monolithic Memories
INCORPORATED
1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535
TWX 910–339-9229

MAY 1974

ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.5 to 7 V
Input Voltage	-1.2 to 7.0 V
Output Current	100 mA
Storage Temperature	-65 to 160°C

Stresses above and extended time at Absolute Maxumim Ratings may cause permanent damage or affect device reliability. Functional operation at these limits in not guaranteed or implied.

D.C. CHARACTERISTICS

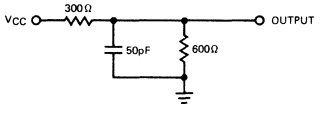
Unless otherwise indicated, all limits for the 6741 are guaranteed for 5 V ±5% in a free air temperature of 0 to 75°C; all limits for the 5741 are guaranteed for 5 V ±10% in a free air temperature of -55 to 125°C.

PARAMETER		CONDITIONS	5741/6741			UNITS
			MIN.	TYP.[1]	MAX.	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45 V			-800	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.40 V			50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 10 mA			0.50	V
V_{OH}	Output Voltage "High"	I_{OH} = -900 μA	2.4	3.2		V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, All Inputs Open (worse case)		100		mA
V_{IL}	Low Level Input Voltage	V_{CC} = 5.0 V			0.85	V
V_{IH}	High Level Input Voltage	V_{CC} = 5.0 V	2.0			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = -5.0 mA		-1.5	-1.0	V
C_I	Input Capacitance	V_{CC} = 5.0 V, V_I = 2.0 V, 25°C, 1 MHz V_{CC} = 5.0 V, V_O = 2.0 V, 25°C, 1 MHz		7.0		pF

1. Typical values are measured at 5.0 V and 25°C.

STANDARD TEST CIRCUIT

STANDARD LOAD



Input Pulse Amplitude = 2.5
Input Rise and Fall Time
5.0 ns From 1.0 V to 2.0 V
Measurements Made at 1.50 V

FIGURE 1

FUNCTIONAL DESCRIPTION:

DATA INPUT:

The four bits of data on the D_0 . . . D_3 inputs are entered into the first bit location when both Input Ready (IR) and Shift IN (SI) are HIGH. This causes IR to go LOW, but data will stay locked in the first bit location until both IR and SI are brought LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

DATA TRANSFER:

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel, from input to the output of a previously empty device.

DATA OUTPUT:

When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of valid data at the output pins Q_0 . . . Q_3. The transfer of data is initiated when both the Output Ready (OR) output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be use as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

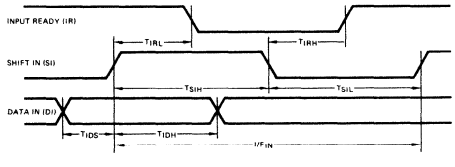
A.C. CHARACTERISTICS WITH STANDARD LOAD (FIG.1)

PARAMETER	SYMBOL	FIGURE	5741/6741 5.00 V, 25°C			UNITS
			MIN.	TYP.[1]	MAX.	
Shift In Clock Rate	F_{IN}	2	10.0			MHz
Shift In High Time	T_{SIH}	2	30			ns
Shift In Low Time	T_{SIL}	2	30			ns
Input Ready Off Delay	T_{IRL}	2		30		ns
Input Ready On Delay	T_{IRH}	2		30		ns
Input Data Set Up	T_{IDS}	2	0			ns
Input Data Hold Time	T_{IDH}	2	30			ns
Shift Out Clock Rate	F_{OUT}	3	10.0			MHz
Shift Out High Time	T_{SOH}	3	30			ns
Shift Out Low Time	T_{SOL}	3	30			ns
Output Ready Off Delay	T_{ORL}	3		30		ns
Output Ready On Delay	T_{ORH}	3		30		ns
Output Data Hold Time	T_{ODH}	3	10			ns
Output Data Delay	T_{ODS}	3			T_{ORH}	ns
Data Thru-Put Time	T_{PT}	Note 2		4.0		μs
Master Reset Pulse	T_{MRW}	Note 3	100			ns
Input Ready Pulse High	T_{IPH}	5	T_{SIH}			ns
Input Ready Pulse Low	T_{IPL}	8	T_{SIL}			ns
Output Ready Pulse High	T_{OPH}	4	T_{SOH}			ns
Output Ready Pulse Low	T_{OPL}	9	T_{SOL}			ns

1. Typical values are measured @ 5.00 V, 25°C.
2. This parameter defines total time from the time data is present at D_0 - D_3 to the time it is available at O_0 - O_3 with FIFO initially empty.
3. Master Reset Clears the 6741 to the all cells empty state.

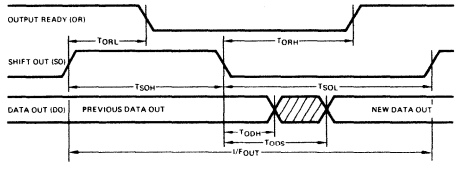
TIMING DIAGRAMS

FIGURE 2
FIFO INPUT TIMING



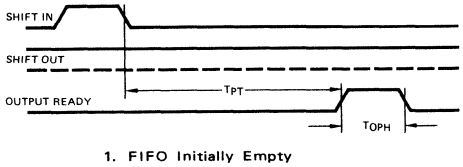
1. Input data must remain stable during T_{IDS} and T_{IDH}.
2. Input Ready HIGH indicates that space is available and a Shift In pulse may be applied. Input Ready LOW indicates that the FIFO is full. Shift In pulses applied while Input Ready is LOW will be ignored.
3. The rise of Input Ready indicates that the data at the D_0 – D_3 inputs has been accepted and that the input stage is empty.

FIGURE 3
FIFO OUTPUT TIMING



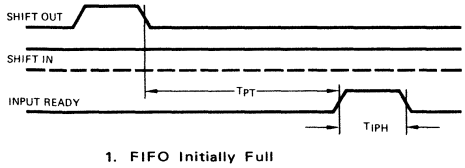
1. Output data will be stable at the rise of Output Ready.
2. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied. Output Ready LOW indicates that the FIFO is empty. Shift Out pulses applied while Shift Out Ready is LOW will be ignored.
3. The rise of Output Ready indicates that new data has been loaded into the output stage.

FIGURE 4
T_{OPH} SPECIFICATION



1. FIFO Initially Empty
2. Shift Out Held High (as shown)

FIGURE 5
T_{IPH} SPECIFICATION



1. FIFO Initially Full
2. Shift In Held High (as shown)

FIRST-IN-FIRST-OUT (FIFO) Serial Memory Operation

GENERAL DESCRIPTION

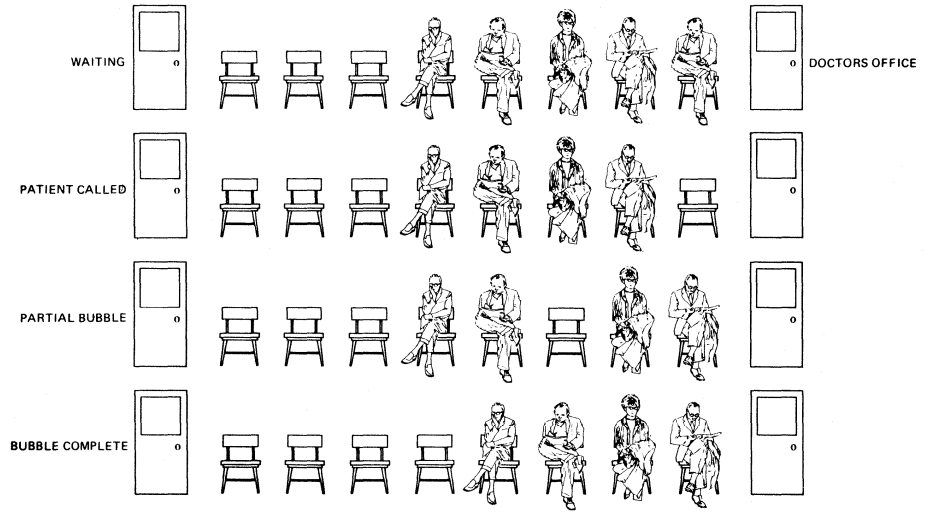
First-In-First-Out (FIFO) memories are used to assemble incoming data at one clock rate to be read out at another clock rate. Examples of this concept include data acquisition systems with magnetic tape output: in these systems, the analog to digital converter (ADC) fills a memory at a constant (20 kHz) rate while the magnetic tape dumps the memory to magnetic tape at high (45 kHz) burst rates.

A simple analogy of FIFO operation is a line of chairs in the waiting room of a doctor's office, as shown in Figure 6. As people enter the waiting room they take the first empty chair nearest the doctor's office, bypassing the other empty chairs. When the doctor calls for the next patient, the person nearest the office leaves his chair. The person next to him moves over and fills his chair, as do the remaining people. The empty chair can be said to "bubble" through the remaining patients, since a waiting patient automatically moves into the empty space nearest the doctor's office.

This situation is obviously dynamic and asynchronous: patients may be entering the waiting room at the same time others are being called into the doctor's office; patients may enter in groups (i.e., families) and/or be called in groups; and a second patient may be called in before the "empty chair" of the first patient has "bubbled" to the end of the line. There may also be a pair of receptionists in this hypothetical doctor's office: one to tell the doctor that there are no patients waiting, and one to tell incoming patients to wait outside because the waiting room is full.

The FIFO Serial Memory operates in a fashion very similar to our hypothetical waiting room. The FIFO is organized as 64 words by 4 bits, which would correspond in our example to 64 benches with each bench 4 people wide, and people entering and leaving in groups of four. In the FIFO, each 4 bit word, or "bench", has an indicator which tells whether that word is full (of good data) or empty. Each word contains logic that detects when it is full and the next downstream word is empty. If this condition exists, the logic automatically loads the data for the word into the empty downstream word, sets the downstream word's full indicator, and clears its own indicator to empty. This is analogous to a person in the doctor's office example detecting that the downstream chair next to him is empty, moving into and filling the empty chair, and leaving his own chair empty. The full/empty logic for each FIFO word operates asynchronously and independently of other words, and is activated only by the current-word-full-next-word empty relationship. The Data Throughout Time, T_{PT}, specification gives the overall time for a new input word to "bubble" through an empty FIFO and reach the output, corresponding to the total time required for a new patient to "bubble" past the empty chairs in an empty waiting room to the chair next to the doctor's office. The FIFO Output Ready indicator corresponds to the receptionist who tells the doctor that there is someone waiting in the last chair, and the FIFO Input Ready indicator corresponds to the receptionist who tells the incoming patients that the seat nearest the door is empty. The input and output clocks correspond to people entering and leaving the waiting room respectively.

FIGURE 6
FIFO ANALOGY: DOCTOR'S WAITING ROOM



SHIFT IN AND SHIFT OUT

The FIFO input and output clocks operate independently and asynchronously of each other. Each clock operates in conjunction with its own ready line. The Shift In and Shift Out high and low times specify the minimum amount of time that the Shift In and Shift Out pins must be high and low, respectively, for reliable operation. The maximum Shift In clock rate is given by F_{IN}; the maximum Shift Out clock rate is given by F_{OUT}.

If the FIFO is empty or partially full, Input Ready, pin 2, will be high indicating that the first FIFO word is empty. If a clock pulse is submitted to Shift In, pin 3, when Input Ready is high, the data present at the data input pins 4-7, will be loaded into the first word by the low-to-high, leading edge transition of the Shift In clock. When the Shift In clock goes high, Input Ready automatically goes low, regardless of the condition of the FIFO. The time delay between the rise of Shift In and the fall of Input Ready is T_{IRL}, Input Ready Off Delay.

When Input Ready is high and Shift In clock goes high, the data on pins 4-7 is loaded into the first word of the FIFO. The data must be stable at pins 4-7 for some set up time before the rise of the Shift In clock. This set up time is T_{IDS} Input Data Set-up time. The input data must also be held stable for some period of time after the rise of the Shift In clock pulse. This time is defined as T_{IDH}, Input Data Hold Time.

FULL

If the FIFO is not full, the fall of the Shift In clock allows the data in the first word to automatically propagate into the FIFO by the asynchronous bubble mechanism described above. When the first word has been loaded into the second word and the first word's full indicator has been cleared, the Input Ready line rises. (However, if the FIFO is full at this point, propagation will not occur, the indicator will not be reset, and the Input Ready line will remain low.) The time delay between the fall of the Shift In clock and the rise of Input Ready for the FIFO not full case is T_{IRH}, Input Ready On Delay.

If the FIFO is full or partially full, Output Ready, pin 14, will be high indicating that the last word in the FIFO is full. If a clock pulse is submitted to Shift, pin 15, while Output Ready is high, the full indicator on the last word will be reset on the leading edge of the clock pulse. When Shift Out pin goes high, the Output Ready line, which indicates the state of the last stage full indicator, goes low. The time delay between the rise of Shift Out and the fall of Output Ready is T_{ORL}, Output Ready Off Delay.

After the fall of Shift Out, the bubble logic is enabled, and new data will be loaded from the next to last word into the last word and appears at the outputs, pins 10-13 (assuming that the FIFO is not empty). After the fall of Shift Out, the output data will remain stable for some period of time and then change to the new data. The Output Data Hold Time T_{ODH}, defines the minimum time that the old output data will remain at the output pins after the high to low transition of Shift Out. The Output Data Delay, T_{ODS} defines the maximum time delay before new data emerges at the output following the high to low transition of Shift Out. The output data lines transition between T_{ODH} and T_{ODS}. After the new data appears at the output, the Output Ready line rises. The time delay between the high to low transition of Shift Out and the rise of Output Ready is defined as T_{ORH}, Output Ready On Delay. (Note that if the FIFO is emptied by the Shift Out clock pulse, Output Ready will not rise until a new word has been entered by Shift In and has bubbled through to the output.)

BUBBLE THRU TIME

The Data Through-Put Time, T_{PT}, defines the time for a new input word to bubble through an empty FIFO from the input to the output. (Note: This time is slightly longer than the time required for an empty location to bubble from the output back to the input.) This time interval, T_{PT}, is defined as the maximum time between the fall of Shift In and the rise of Output Ready for a previously empty FIFO.

RESET

Master Reset, pin 9, resets all full indicators for all words to the empty state. This subsequently forces Output Ready low and Input Ready high. It is typically used at system power up to clear the FIFO to the empty state. The Master Reset Pulse Width, T_{MRW}, defines the minimum time the Master Reset pin must be low to accomplish this function.

The Master Reset function clears the control latches for all FIFO cells to the empty state. The contents of the corresponding data locations are unaffected: i.e., a Master Reset pulse will not affect data present at the FIFO outputs. To clear all FIFO data to all zeros, 64 words of all zero's must be shifted into the FIFO after Master Reset. To clear the output data only to zero, one word of all zeros must be loaded after Master Reset.

Both Shift Out and Shift In lines should be held low during Master Reset. Otherwise, when Master Reset is removed, the input logic will see an effective negative-to-positive, leading edge transition of Shift In if Shift In was held high during Master Reset. (The output logic will not be effected since Output Ready cannot go high because all control latches were cleared by Master Reset.)

EXPANSION

FIFO's can be connected serially to form larger effective FIFO's: i.e., two 64 x 4 FIFO's can be connected to form a 128 x 4 FIFO, as shown in Figure 7. This is done by connecting the data outputs of the input side FIFO, A, to the data inputs of the output side FIFO, B, and Output Ready and Shift Out pins of the input FIFO, A, to the Shift In and Input Ready pins of the output FIFO, B, respectively. Figures 8 and 9 show a 192 x 12 FIFO and how to generate composite input ready and output ready signals.

FIGURE 7
128 x 4 FIFO

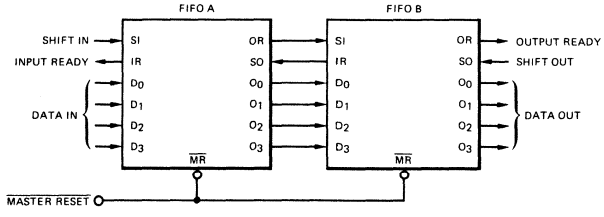


FIGURE 8
192 x 12 FIFO – UNLATCHED CONTROL LINES

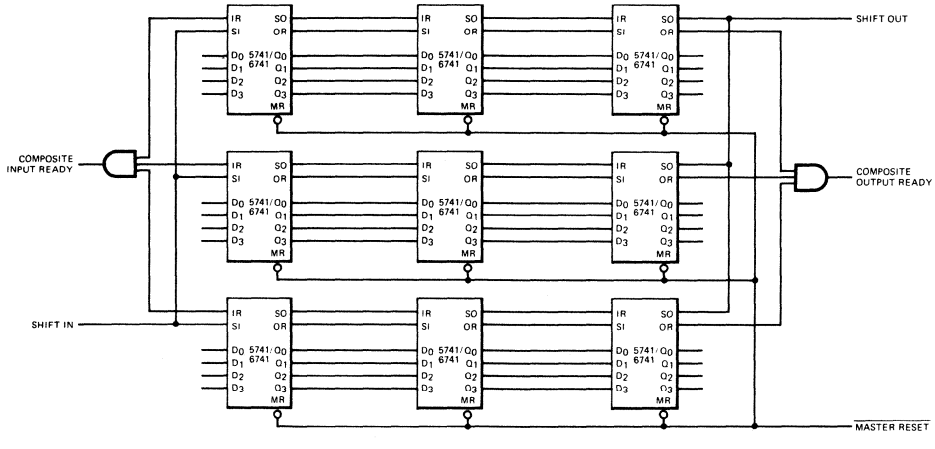
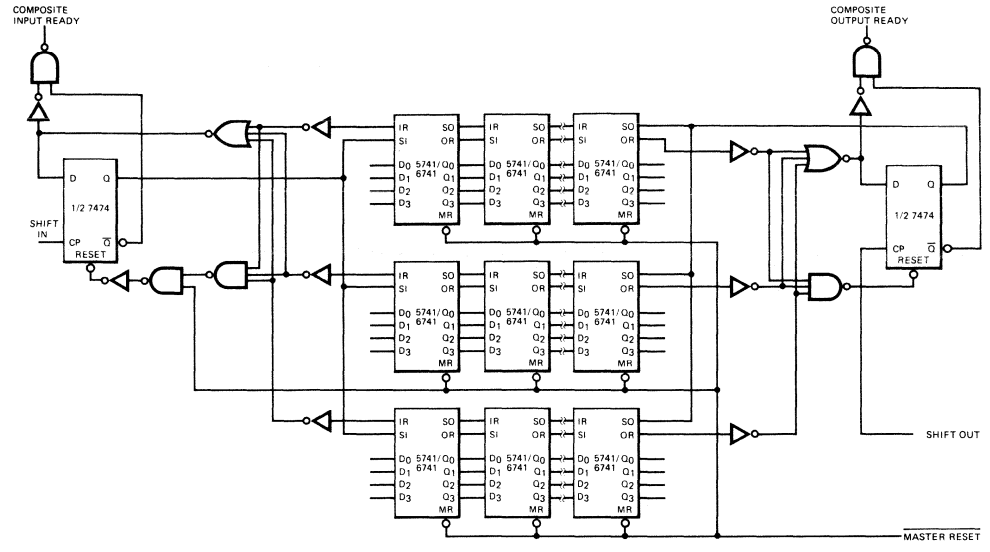


FIGURE 9
192 x 12 FIFO – LATCHED CONTROL LINES



If both FIFO's are empty, the Input Ready/Shift Out pins between the FIFO's will be high and the Output Ready/Shift In pins between the FIFO's will be low. If the Shift In pin of FIFO A is clocked, the data will propagate to the output. This will set the output full indicator, causing the Output Ready/Shift In combination to rise temporarily. However, since the Input Ready/Shift Out combination is high this enables the Shift Out clock and the full indicator is reset immediately after the rise of Output Ready/Shift In. The result in a positive going pulse on the Output Ready/Shift In line which is T_{OPH}, Output Pulse High (empty), as shown in Figure 10. The FIFO chip is designed such that this pulse is greater than the minimum Shift In high time, T_{SIH}. The leading edge (low to high) of this Output Ready pulse indicates that the new word is available at FIFO A's output. This low to high transition on FIFO B's Shift In line causes FIFO B to load the data from FIFO A into B's first (input) word. FIFO B responds by taking the Input Ready/Shift Out combination low. The trailing edge, high to low transition of Output Ready/Shift In Pulse allows the word in FIFO B to propagate on to its output. Once propagation has begun, FIFO B will again raise Input Ready/Shift Out. The result is a negative pulse on the Input Ready/Shift Out line which is T_{IPL}, Input Pulse Low (empty). The FIFO is designed such that this pulse is greater than the minimum Shift Out low time, T_{SOL}.

FIFO TO FIFO COMMUNICATION

Chip to chip communication for the case of two connected FIFO's, both full, with an empty location bubbling from the output to the input is similar to the both-empty case described above. When both FIFO A and B are full, Input Ready/Shift Out is low and Output Ready/Shift is in high. When an empty location bubbles from the output of FIFO B to its input, Input Ready/Shift Out will temporarily go high. Since Output Ready/Shift In is already high, the Shift In clock is enabled and Input Ready/Shift Out will immediately go low. The result is a pulse on the Input Ready/Shift Out line which is T_{IPH}, Input Pulse High (full), as shown in Figure 11. The FIFO is designed such that this pulse is greater than the minimum Shift Out high time, T_{SOH}. The leading edge of this pulse will cause FIFO A to load new data at its outputs, and the trailing edge will cause the newly created empty location to bubble through FIFO A. The rise of the Input Ready/Shift Out pulse will cause Output Ready/Shift In to go low. Output Ready/Shift In will go high again when new data has been loaded into FIFO A's output. This creates a negative pulse on the Output Ready/Shift In line which is T_{OPL}, Output Pulse Low (full). The FIFO is designed such that T_{OPL} is greater than the minimum Shift Out low time.

FIGURE 10
FIFO/FIFO COMMUNICATION: EMPTY/INPUT TIMING

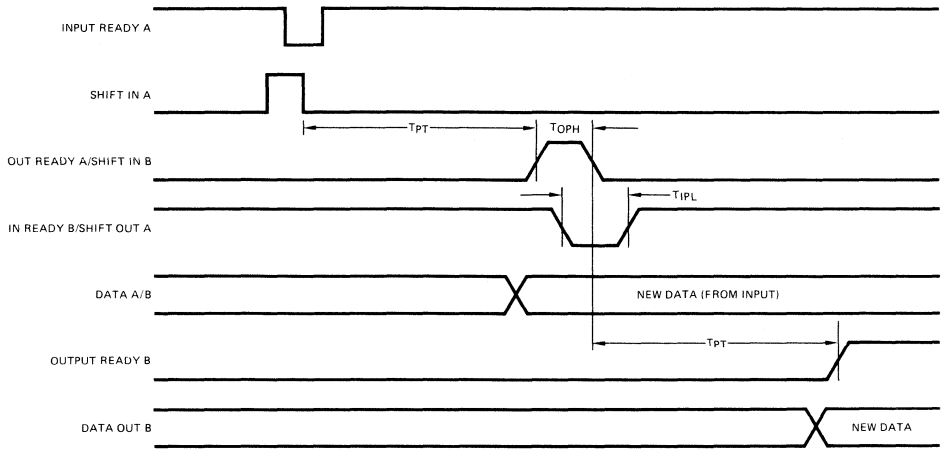
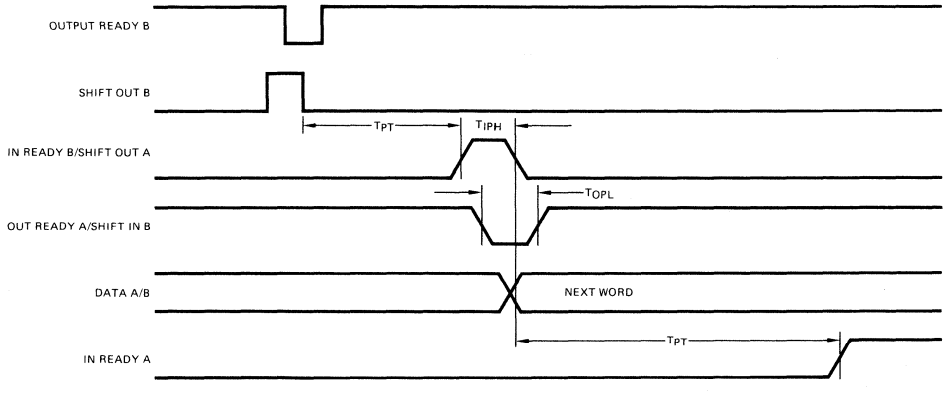


FIGURE 11
FIFO/FIFO COMMUNICATION: FULL/OUTPUT TIMING



PROGRAMMABLE READ ONLY MEMORY RELIABILITY REPORT II

Monolithic Memories
INCORPORATED

April 1, 1974

The Programmable Read Only Memory is a unique semiconductor device in as much as it is the first product that the manufacturer has passed a few of the final testing steps on to his customer. These are, of course, the programming and subsequent final testing of the device. Many users of Programmable ROMS have not recognized all the ramifications of these operations and perhaps more significantly the related quality and reliability issues.

Monolithic Memories, Inc. constantly strives to reduce this source of confusion by continually improving the quality of the product and by advancing the state-of-the-art PROM technology.

One factor which has not been entirely overcome is a method to 100% predict the success or failure of each fuse in every device before actual programming. We have, however, come a long way on the learning curve and are currently focusing on the last few percent. (See Figure #1).

These areas of PROM usage require attention:

(1) Programming Technique
(2) Verification and testing after programming
(3) Early mortality failures during the first hours of operation
(4) Long term reliability

Programming: Several phenomena associated with programming are, mis-programmed fuses, those that won't program and slow programming devices. Together these account for most of the programming yield loss.

Mis-programming is chiefly due to internal breakdowns or leakage paths providing access to multiple fuse locations. This has been reduced in current MMI PROM designs by special in-process testing and lowering the required programming voltage at the output. In the past, misprogramming was partially due to our inability to perform a complete

decoding check at the package level on an unprogrammed device. Although extra test "word" and "bit" lines were incorporated on the chip, they were only accessable through extra probe pads on the die itself, and could not be bonded out in the package form for lack of sufficient pins. This problem was overcome in the current designs by using an advanced multiplexing concept in two of the input pins enabling MMI to check decoding on the package level as well as at wafer sort. This feature also allows access to a pattern of test fuses which are blown on the package level to check out the programming characteristics of each device. One input pin also allows V_{OL} testing on the unprogrammed device by turning on all four outputs.

Fuses that won't program usually reflect an internal circuit leakage or breakdown condition shunting the necessary programming current away from the selected fuse. Devices which program very slowly* usually exhibit a similar lack of programming current for much the same reasons but the condition is only marginal.

The occurence of these phonomena have been greatly decreased in the current revision by improving the design, reducing the die size, and implementing special in-process tests.

Verification: After successful programming the device should be tested to see that it conforms to the entire device electrical specification. High programming voltages may have accelerated the failure of marginal components in the circuitry. Therefore, after final testing one might expect some small additional fall out, usually less than 1%.

Early mortality fallout, that fraction of the devices failing during the early hours of operation, may be grouped into three categories:

(1) 80-95% of the initial population of devices will exhibit Input/Output shorts; sometimes due to stressing a defective component in the circuit during programming

(2) 5-15% Mechanical Failures: typically assemmbly oriented workmanship defects

(3) 1-5% "Grow-Back"; where improperly programmed fuses change resistance value due to dendritic relinking

* This is relative for each programmer and its pulse train. Using the MMI 530 Programmer units requiring over four minutes are considered slow.

It is important to note that the combined early mortality failure modes only account for ~1% of the product, a figure much less than many conventional integrated circuits. Typical incidence vs. time to failure is represented in Figure #2.

The first two modes are readily understood and I will not pursue them any further except to say that our Process Control efforts are constantly improving the rarity of such events.

"Grow-Back" was first used as a term to describe the apparent reversal of the programming process. An output would appear to go from the programmed low state back to an unprogrammed high state. Most device failures of this sort involved only one fuse. Those that exhibited multiple fuse failures usually were found to be cases where a multiplex transistor had shorted and a whole bit line or word line would be involved. Obviously, these latter failures did not reflect a failure in the fuse but in the decoding circuitry. The true "Grow-Back" failure is presently a very rare occurrence with Monolithic Memories product and have never been experienced in life-testing that was performed after suitable screening procedures consistant with Level B processing of Method 5004.1, MIL-STD-883.

The purpose of this bulletin is to clarify this phenomenon. It should be emphasized that this study on "Grow-Back" was isolated from other reliability studies for two reasons:

(1) The phenomena has proven under controlled experiment, as well as in the field to be an early mortality failure and does nc appear to impact the long term life (MTBF) of the device.

(2) Since it is a new failure mechanism indigenous to nichrome fuse PROM's, much interest, speculation and misinformation has been generated in the field.

I CHARACTERISTICS OF "GROW-BACK"

In our failure analysis lab we have extensively examined devices which have failed in this mode. Normally blown fuses usually display resistance $>$ 2 megohms. Careful probing through silox passivation to the aluminum on either side of the grow-back fuse has shown us that all of the failing fuse resistance values fall between 900 and 2000Ω., Figure #3. This is much higher than the ~ 350Ω value for an unprogrammed fuse. The output load characteristic was found to reflect this "twilight" fuse resistance region by sometimes appearing "on" (logic low) at high V_{CC} and/or high temperature and "off" (logic high) at low V_{CC} at low temperature. Varying the load on the output also had an effect on this transition from one state to another. Figure 4b shows the V/I characteristic of the fuse at a failing address #87, output #1. The resistance was 1K . After silox removal and scanning electron microscopic analysis, Figure #5, the fuse was re-blown requiring a typical 0.90 mA. Generally an unprogrammed fuse starts out at a resistivity of ~ 350Ω and requires 14-16 mA blowing current. Another fuse in the same device was examined, Figure 4a, and shows the normal V_{OL} characteristic over V_{CC} excursions. The SEM analysis of this fuse using a voltage contrast mode exhibits a clean opening with no leakage as indicated by the sharp break in the contrast in the fuse gap region, Figure #6. Note in the fuse that failed, Figure #5, dentrites bridge the gap and a uniform contrast across the fuse indicates that both sides are at the same potential. The most significant point is that the device which failed will operate correctly at and above a V_{CC} of 5.20 volts. This transition voltage has been observed as low as 4.3 volts at room ambient, 25°C. Thus, it becomes evident that some sort of low temperature or low V_{CC} test is necessary to detect this type of failure. If by chance, you are near the transition on some devices, the failure mode might appear as an oscillating bit such as the characteristic in Figure #7. The reason for these V_{OL} effects is simple; the sense circuitry threshold levels overlap the region of "Grow-Back" fuse resistivities.

II CAUSE OF THE PHENOMENA

During the investigation as to why fuses failed in this particular mode, we monitored many variables, but only one was consistently linked with "Grow-Back" failures, programming difficulty. Parts that would program very slowly (4-5 minutes) and which heated up in doing so, would invariably have a higher incidence of failure, up to 2-3%.

In order to study the phenomena further, we designed a test chip, Figure #8, in which fuses processed identically to the actual device are bonded to outside package pins. This enabled us to directly vary programming conditions at the fuse and monitor probability of "Grow-Back" under different stress conditions. The results are summarized:

1. Fuses that "Grow-Back" do so only under the inducement of a voltage potential across the gap region of the fuse within a few volts of the breakdown voltage of that gap.

2. Temperature cycling or high temperature storage did not induce failure and, therefore, cannot be used to screen out potential failures.

3. Most failures occur within the first 100 hours @ room ambient under a stress of a few volts.

4. The "Grow-Back" fuses are always around 1000-2000Ω and easily re-blown at currents typically below 1.0 mA.

5. The higher the breakdown voltage of the gap, the lower the probability that "Grow-Back" can ever take place no matter what potential is applied across the gap. Above a 20 volt breakdown the effect virtually disappears. Blown fuses that demonstrate subsequent low voltage breakdowns in the gap region, around 0.5-2.0 volts, invariably grow back, when a field is applied, sometimes in milliseconds.

6. Limiting the rate at which programming current is available would always cause fuses to exhibit very low breakdown voltages across the gap region. This phenomena is illustrated by programming fuses with slow rise times on the voltage pulse, Figure #9, and #16.

7. On fuses that opened on a fast rise time pulse $< 10\mu$ sec, the fuse resistance approached infinity almost instantaneously, Figure #10, whereas slow rise-time pulses $>$ 20 msec, exhibited an unstable slow decay characteristic lasting some 4 msec, Figure #11. The latter was generally associated with fuses that had a high probability of "Grow-Back" under an applied field. SEM inspection of such fuses exhibit unremoved metal in the gap regions, Figure #12.

8. Fuses without silox, exposed to air could <u>never</u> be blown slow enough to give low breakdowns in the gap region or display the attendant "Grow-Back" phenonemon. This suggested that oxidation may be an important mechanism of programming.

9. Fuses without silox exposed to forming gas, Nitrogen-Hydrogen mixture, a reducing atmosphere, grew back much more easily than those with silox under similar programming conditions. This supports the contention that oxidation plays an important part in the blowing mechanism at high $\frac{dE_p}{dt}$*, i.e., fast blowing conditions.

The implications of these observations were extrapolated using actual devices in an exhaustive product engineering analysis that led us to these observations:

1) The devices which failed in the "Grow-Back" mode exhibited either a current limiting condition within the PROM circuitry or were current limited by the programming equipment. In any case, a definite correlation with limited programming energy was observed.

2) The maximum voltage across a fuse during normal operation would be no more than 2.9 volts and this would occur only at a V_{cc} of 5.5 volts and only when certain bits were addressed. Not every blown fuse would see this stress level unless all addresses were clocked using a counter or some other random pattern generator.

3) It followed that the best screening for surfacing potential "Grow-Back" failures was a dynamic burn-in at maximum rated V_{cc} and at maximum rated operating temperature. Detection of the failures would be best accomplished by using a low $V_{cc} \sim 4.2V$ and a high I_{ol} (output load of 12 mA while performing a functional parity check.

---

* E_p = Programming energy

t = Programming time

4) Devices should characteristically program on the rise time of the pulse if there is no current limiting factor. If the fuse does not program then, higher voltages should be tried to overcome the current limiting condition. Longer pulses would only serve to raise the programming energy by slowly raising the ambient temperature and this has been shown to have a similar effect as slow rise time of the voltage pulse; both contribute to low breakdowns in the gap region and invite "Grow-Back" failures.

5) The rise time of the programming pulse should not exceed 100 μ seconds.

6) The device oriented mechanisms which limit current to the fuse were:

a) Low breakdown on reverse biasing of junctions which normally prevent programming current from flowing in unwanted paths.

b) Failure of circuit designs to assure sufficient programming current under worse case conditions encountered in process variations. See Figure #13.

c) Low beta such that the multiplex transistor was no longer capable of supplying sufficient current. See Figure #14.

d) Random defects simulating above conditions (a,b,c)

III CORRECTIVE ACTION

Concurrent with the program discussed above, MMI introduced a comprehensive program to correct the discrepancies as they were uncovered in the Reliability, Failure Analysis and Product Engineering investigations The action taken is outlined:

1. All PROM products were redesigned to maximize programming current available within the circuit over a well defined process. Programming voltages were lowered away from the limiting value of the breakdown of reverse biased outputs $\sim$ 30-38 volts to 20-26 volts.

2. Increased process controls were established to keep product within the defined process limitations.

3. Measures (proprietary) were taken to reduce random defect count and density.

4. Special diagnostic tests for factors that limit programming current were installed at wafer sort and package final testing.

5. During the redesign phase, extra word and bit lines were put into the larger PROM devices providing extra fuses that were used for complete decoding checks on both chip and package level tests. This approach also permits worse case V_{ol} testing on the unprogrammed device

as well as supplying worse case test fuses for programming checks. In addition AC testing can be performed before programming. These are all accomplished on the package level by taking certain address pins up to ~ 11 volts, breaking down a zener which then makes the additional circuitry available.

6. Programming specifications have been optimized for reliable programming. (Appendix B)

7. For Level-B Military screening to MIL-STD-883, a dynamic burn-in capability has been added in-house, Figure #15.

8. Every unprogrammed device shipped has passed test-fuse programming.*

9. Our reliability department constantly monitors fluctuations in early mortality distributions of all PROM's and proves the device reliability by further life testing. (Appendix A)

10. An intensive study of programming mechanisms as well as a quantitative analysis of the "Grow-Back" phenomenon is in progress in order to further define boundary conditions for PROM design, manufacture and programming.

V CONCLUSION

It is evident, not only from our studies, but those of other independent researchers, that "Grow-Back" is a field induced mechanism wher metal dendrite formation occurs in the gap region of a blown fuse. It has been shown that the phenomena is limited to fuses blown such that the breakdown voltage of the gap region is a low 2-5 volts, and does not appear in fuses with high breakdown voltages.

The study of "Grow-Back" phenomena has provided the following results:

1. The phenomena appears as an early mortality failure mechanism and does not impact long term life (MTBF) of the device. Field experience of billions of device hours support this contention.

2. Potential early failures can be removed effectively by use of a dynamic burn-in at maximum temperature and V_{CC} followed by a special functional test.

3. New revisions of all the PROM family have been made taking advantage of our studies and the resulting devices have shown impressive preliminary performance results over their earlier predecessors with virtual elimination of the "Grow-Back" phenomena. (See Figure #1, June '73 and Appendix A)

* Except the 256 bit PROM which due to the simpler and smaller amount of decoding circuitry, did not make extra fuses effacacious.

Further study of the kinetics of the "Grow-Back" mechanism are continuing by gathering data at accelerated conditions in order to determine activation energies. Programming studies are continuing along similar lines in order to characterize the mechanism of programming at both low and high values of $\frac{dE_p}{dt}$.

Our present data suggests a model whereby fast blowing conditions, i.e., high $\frac{dE_p}{dt}$, cause the fuse to open by a rapid oxidation reaction with silox producing narrow fuse gaps with characteristically high breakdown voltages and high resistance to "Grow-Back". Slow blowing conditions, i.e., low $\frac{dE_p}{dt}$, appear to favor an electromigration or "meltback" like opening mechanism which characteristically leaves a network of islands or filaments of nichrome metal in a wide gap region typically exhibiting low breakdown voltages and increased probability of "Grow-Back" when a voltage potential is applied across the fuse gap. See Figure #12. Detailed physical and chemical analysis of the gap region to substantiate this model has been difficult due to the small gap widths involved, 1-5K Å, which are outside the realm of normal spectroscopic methods. We are currently exploring some state-of-the-art analytical tools and results will be made available when practicable. MMI believes that we have established reasonable boundary conditions to avoid the phenomenon while simultaneously improving upon the programming yield, performance and quality of our PROM's.

Paul G. Franklin

Reliability Quality Assurance Manager

LEVEL"B" -883 SCREENING FAILURES

APPENDIX A

TABLE I

DEVICE	QTY	Early Mortality Failures Qty	%	"Grow-Back Failures" Qty	% Total
Old 1K-Prom (5300A)	4117	52	1.3%	4	.10%
New " (5300/1D)	8232	68	.83%	1	.012%
(Improvement Factor)**			1.6X		8X
ld 2K-Prom (5305B)	918	35	3.8%	22	2.40%
ew " (5305/6D)	3216	31	.96%	1	.031%
(Improvement Factor) **			4X		80X
ld 256-Prom (5330B)	416	5	1.2%	1	.24%
ew " (5330/1C)	2007	9	.45%	0	0
(Improvement Factor) **			2.7		*
ld 4K-Prom (5340)	210	7	3.3	2	.95%
ew " (5340)	817	18	2.2	0	0
(Improvement Factor)**			1.5X		*

Discussion: This table represents total rejects after 168 hours of dynamic burn-in @125°C and subsequent post burn-in testing. Burn-in diagram's per Figure #15.

Quantities under "Grow-Back Failures" represent the number of total devices failing for this failure mode.

Note the improvement factors between old and new device designs with respect to all early mortality failures and "Grow-Backs". It becomes evedent that "Grow-Back" is now an insignificant failure mode and that the total early mortality distribution has been brought down to on the average of less than 1%.

* Sample sizes are considered too small a sampling upon which to base an accurate improvement factor.

Improvement Factor: Number of times (X) is the reduction factor.

TABLE II LIFE TEST DATA

for 1K & 2K Proms

	Qty. Devices Tested	Burn-In Cond. [1]	Total Hours	Total Device Hrs.	# Failures	Comments
5300A	76	C	5000	380K	0	
"	105	C	2500	262.5K	0	
"	132	D	5000	660K	1	2
"	105	D	2500	262.5K	0	
"	250	C	1000	250K	2	3
		Total Device Hrs.		1,815K		
5300D	76	D	5000	380K	0	
5301D	76	D	5000	380K	0	
5300D	105	D	2500	262.5K	0	
"	105	D	5000	525K	1	4
"	105	D	1500*	157.5K	0	
		Total Device Hrs.		1,705K		
5305B	45	C	5000	225K	2	5
"	76	D	1000	76K	0	
"	105	D	2500	262.5K	1	6
		Total Device Hrs.		563.5		
5305D	45	C	5000	225K	0	
5305D	105	D	2500	262.5K	0	
5306D	76	D	1000	76K	0	
5305D	105	D	5000	525K	1	7
5305D	105	D	2000*	210K	0	
		Total Device Hrs.		1,298.5K		

1. Condition C represents reverse bias and power and uses the circuit shown in Figure 14B. This was performed @ 125°C. Condition D, also @ 125°C is a dynamic stress with outputs loaded as shown in Figure 15. All units were burn-in screened for 168 hours per Level B MIL-Std-883 Test Method 5004.1. In all cases ½ of the bits were programmed.
2. This device failed @ the 168 hour end point test due to increased output leakage. Although this device is a marginal drift reject it would not have failed in actual use since the device stabilized and still meets the 40 μA leakage specification.
3. Both failures occurred @ the 168 hour end point test. One unit failed input leakage marginally.

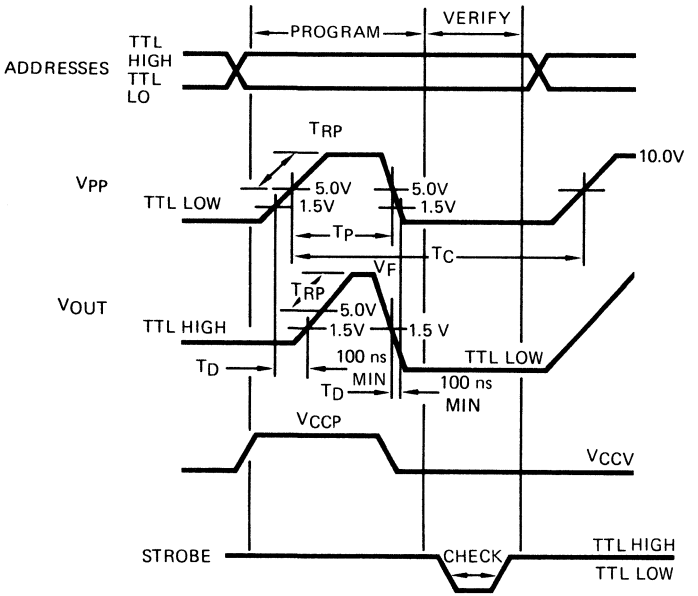
   The other device failed input leakage also but on the programming pin (#13).

4. Device failed enable pin leakage at 168 hr, reading as a short.

5. & 6. All failures were output leakage drift failures at 168 hrs, two remained in specification while the other continued to drift out of specification with additional burn-in.

7. This device failed operation at the 504 hr reading as an open. Failure analysis showed one of the bonds, V_{CC}, melted open. This was attributed to an overstress condition probably arising from a device being loaded into the test socket backwards.

PROGRAMMING PARAMETER



SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS MIN.	LIMITS TYPICAL OR OPTIMUM	LIMITS MAX.	UNITS
I_{pp}	Current into Program Pin During Programming, Before and After Fuse Has Blown	V_{CC} = 5.50 V V_{out} = 5.0 V to 25 V V_{pp} = 4.50 V		0		mA
		V_{pp} = 29 V		150		mA
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{pp} = 29 V, V_{CC} = 5.50 V V_{out} = 9.0 V		0.1		mA
		V_{out} = 20 V		16		mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{pp} = 29 V, V_{out} = 20 V V_{CC} = 5.50 V		10		mA
T_{RP}	Rise Time of Program Pulse Applied to the Data out or Program Pin From 5 V to 20 V		10.0	20±10	100	µs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
V_{CCV}	V_{CC} Required During Verification	Both Chip Enables Low	4.10	4.20	4.30	V
I_{OLV}	Output Current Required to Guarantee a Fully Programmed Link	T_A = 25°C, V_{CC} = 4.20 V	12			mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	T_P T_C			25	%
V_{pp}	Required Programming Voltage on Program Pin		28		34	V
V_{out}	Required Programming Voltage on the Output Pin		20		26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{pp} = 33 V V_{out} = 25 V V_{CC} = 5.50 V	240			mA
T_p	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		0.040		300	ms
T_D	Required Time Delay Between Disabling the Memory Output and Application or Removal of the Output Programming Pulse (see Item 4, page 4)	Measure at 1.5 V Levels	100			ns

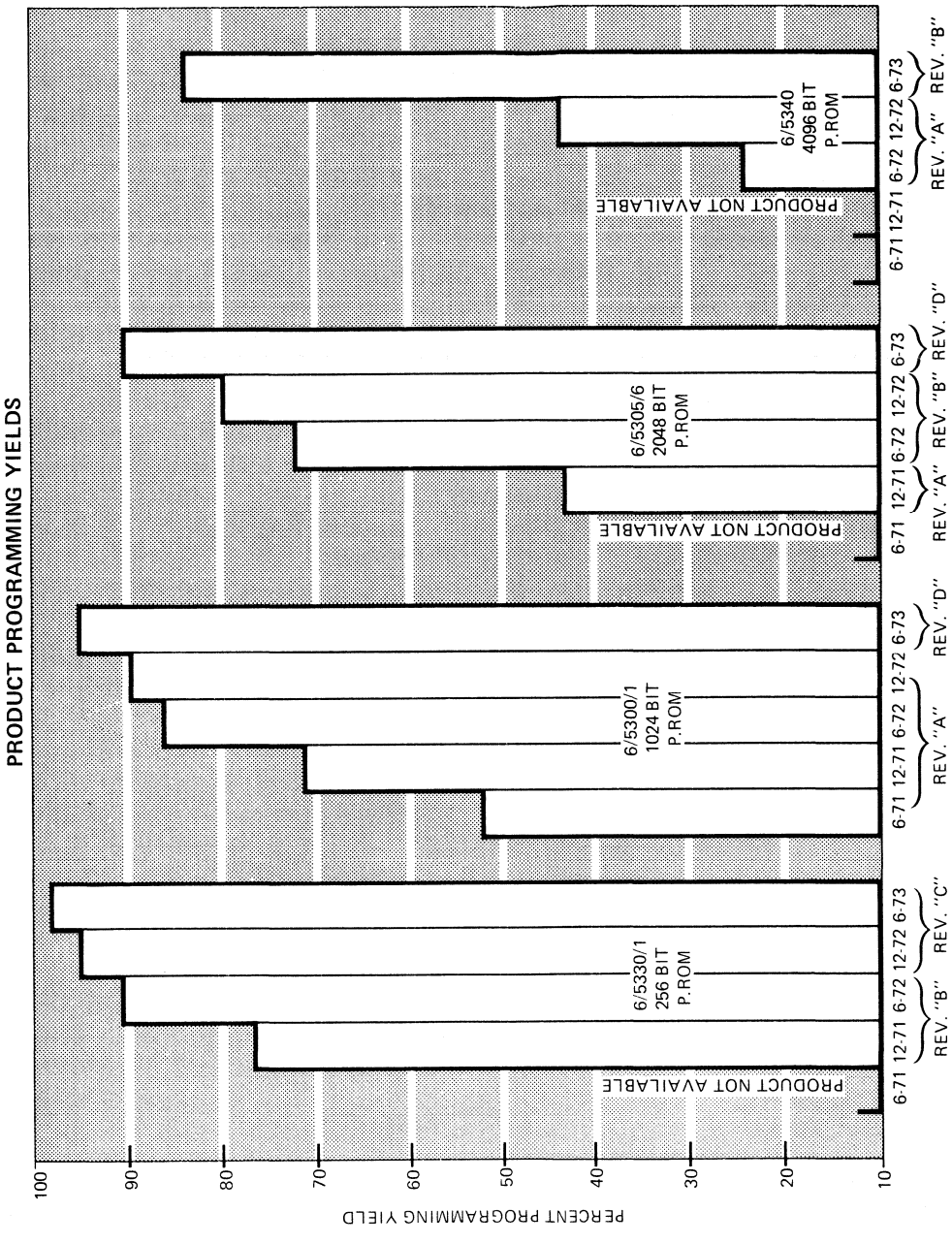

PRODUCT PROGRAMMING YIELDS
PERCENT PROGRAMMING YIELD
100
90
80
70
60
50
40
30
20
10
6/5330/1
256 BIT
P.ROM
6/5300/1
1024 BIT
P.ROM
6/5305/6
2048 BIT
P.ROM
6/5340
4096 BIT
P.ROM
PRODUCT NOT AVAILABLE
6-71 12-71 6-72 12-72 6-73
REV. "B" REV. "C"
REV. "A" REV. "D"
REV. "A" REV. "B" REV. "D"
REV. "A" REV. "B"

FIGURE 1

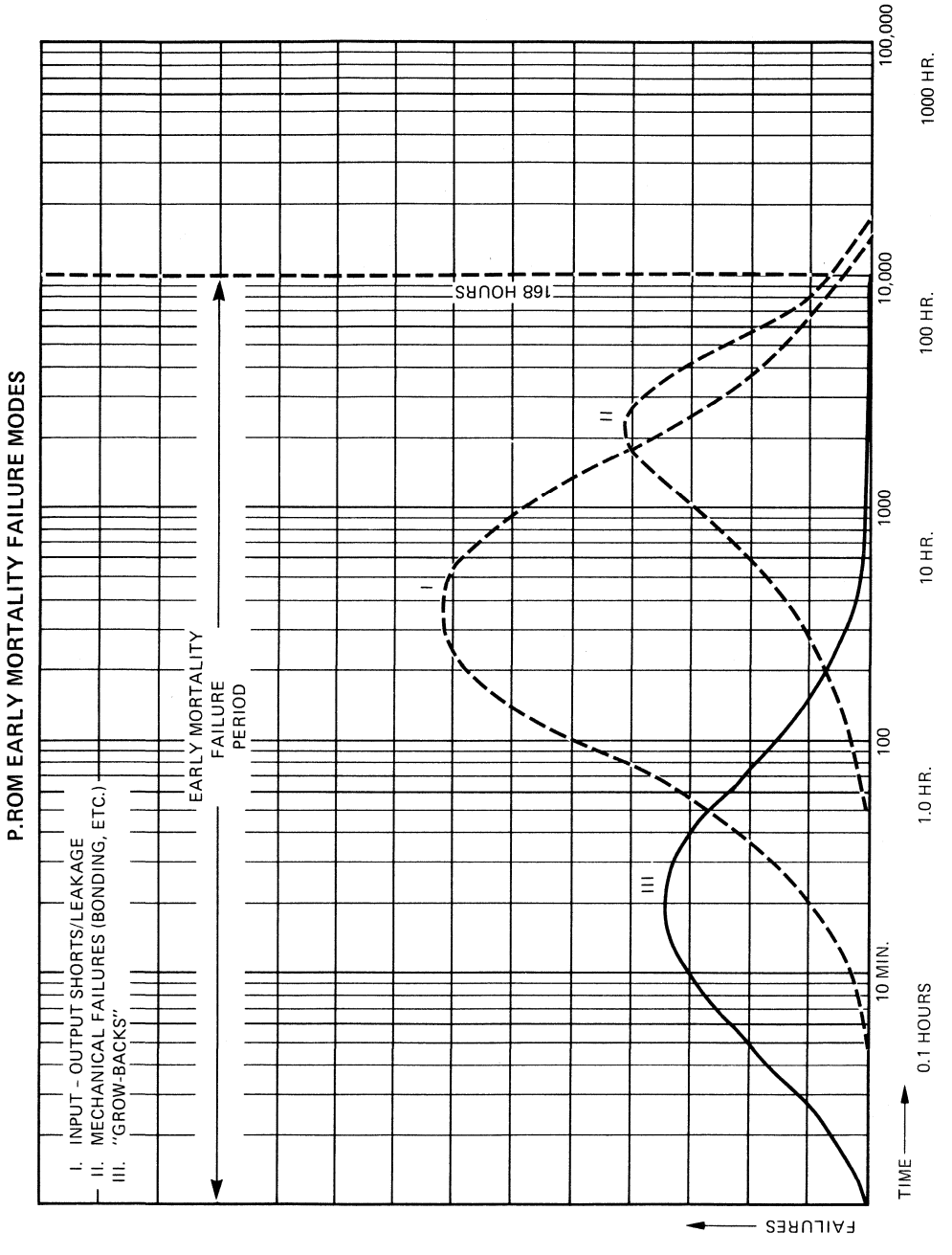

P.ROM EARLY MORTALITY FAILURE MODES
I. INPUT - OUTPUT SHORTS/LEAKAGE
II. MECHANICAL FAILURES (BONDING, ETC.)
III. "GROW-BACKS"
EARLY MORTALITY FAILURE PERIOD
168 HOURS
I
II
III
FAILURES
TIME
0.1 HOURS
10 MIN.
1.0 HR.
100
10 HR.
1000
100 HR.
10,000
1000 HR.
100,000

FIGURE 2

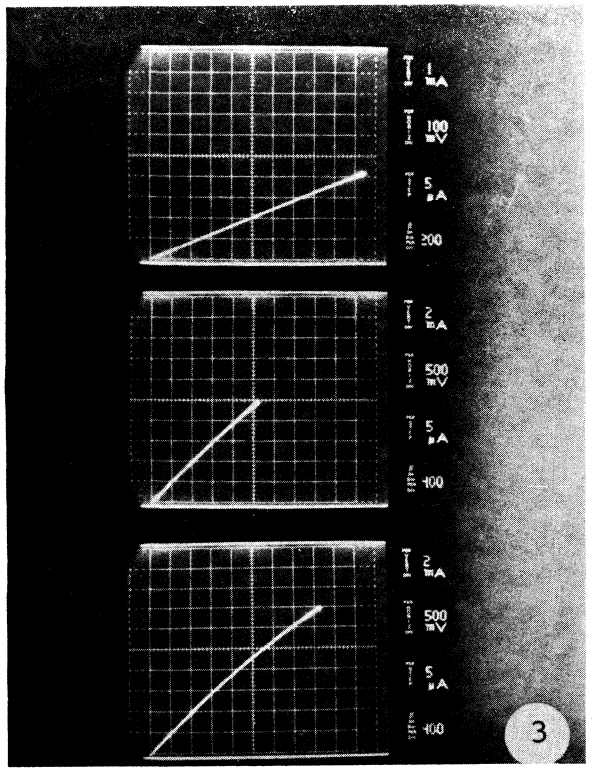


FIGURE 3A

RESISTANCE V/I CHARACTERISTIC OF A NORMAL ~ 250Ω FUSE; BLOWN AT 14.5 mA @ 4.5 V.

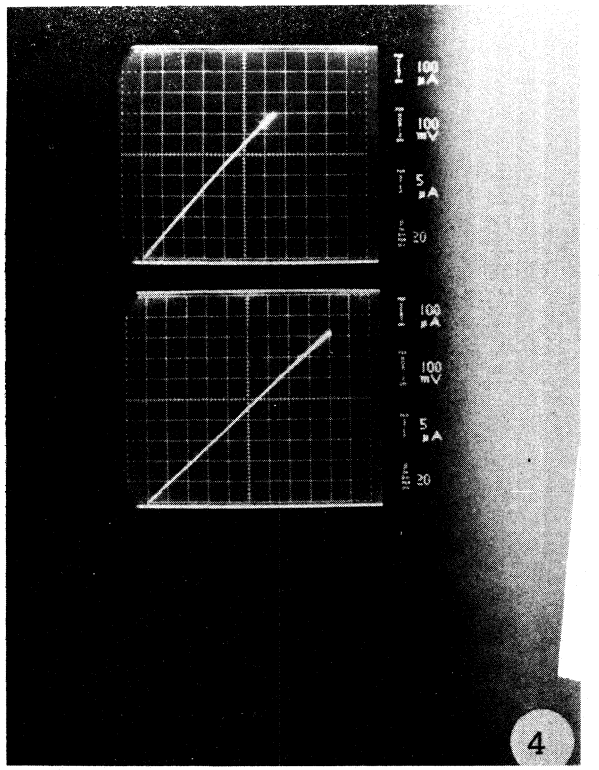


FIGURE 3B

RESISTANCE V/I CHARACTERISTIC OF A FUSE WHICH "GREW BACK" ~ 1000Ω; REBLOWN AT 0.9 mA @ 1.0 V.

NOTE: NORMALLY BLOWN FUSES HAVE RESISTANCE VALUES ABOVE 2 MEG OHMS @ ~ 5.0 V.

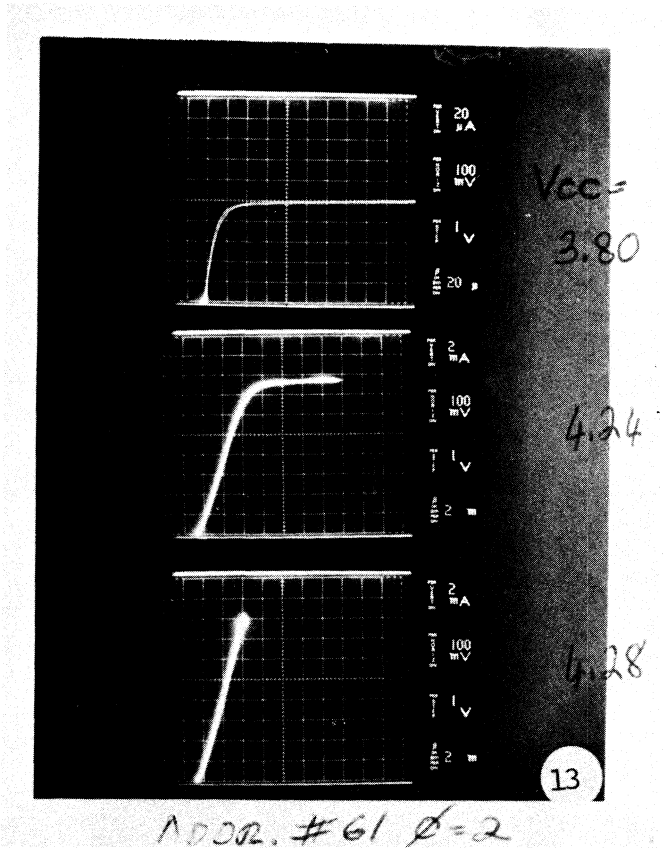


FIGURE 4A

V_{OL} / I_{OL} CHARACTERISTIC OF A NORMAL OUTPUT HELD AT AN ADDRESS WHERE THE FUSE WAS BLOWN PROPERLY. NOTE THAT THE OUTPUT DOES NOT GO OUT OF SATURATION UNTIL ~ 3.8 VOLTS V_{CC}.

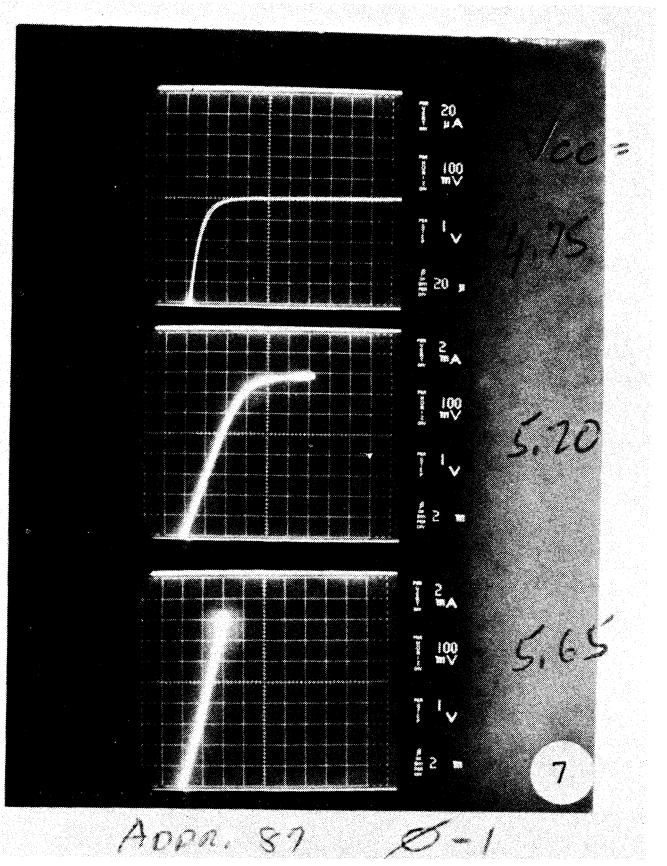


FIGURE 4B

V_{OL} / I_{OL} CHARACTERISTIC OF AN OUTPUT HELD AT AN ADDRESS WHERE THE ORIGINALLY PROGRAMMED FUSE "GREW BACK". NOTE THAT THE OUTPUT IS ALREADY OUT OF SATURATION (TURNED OFF) AT A V_{CC} OF 4.75 VOLTS.

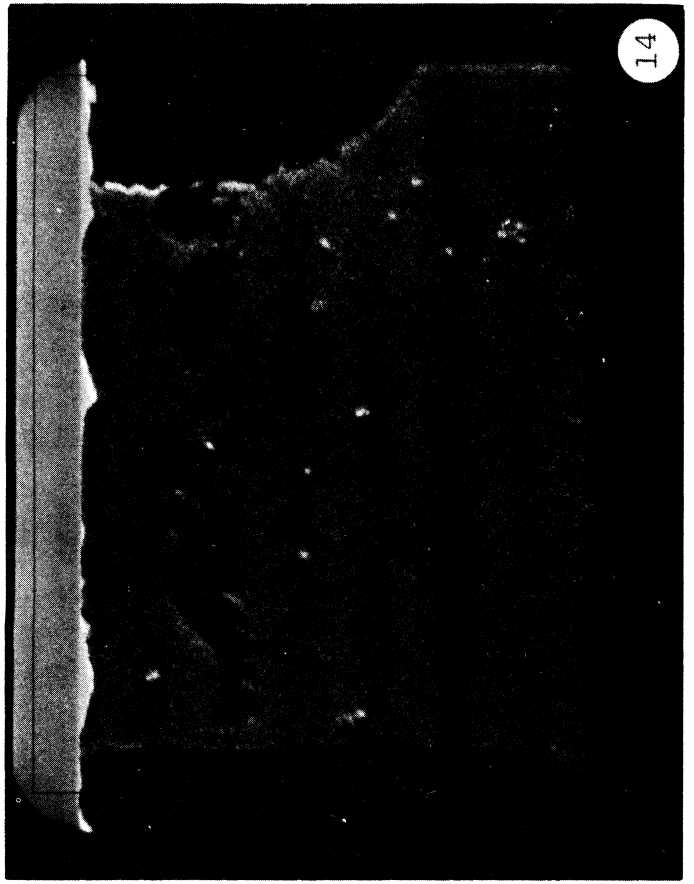


FIGURE 5

SEM PHOTO (12,000X) USING VOLTAGE CONTRAST OF A FUSE WHICH HAS "GROWN BACK". NOTE THE FILAMENTS BRIDGING THE GAP REGION AND THE LACK OF CONTRAST BETWEEN THE TWO SIDES OF THE GAP REGION.

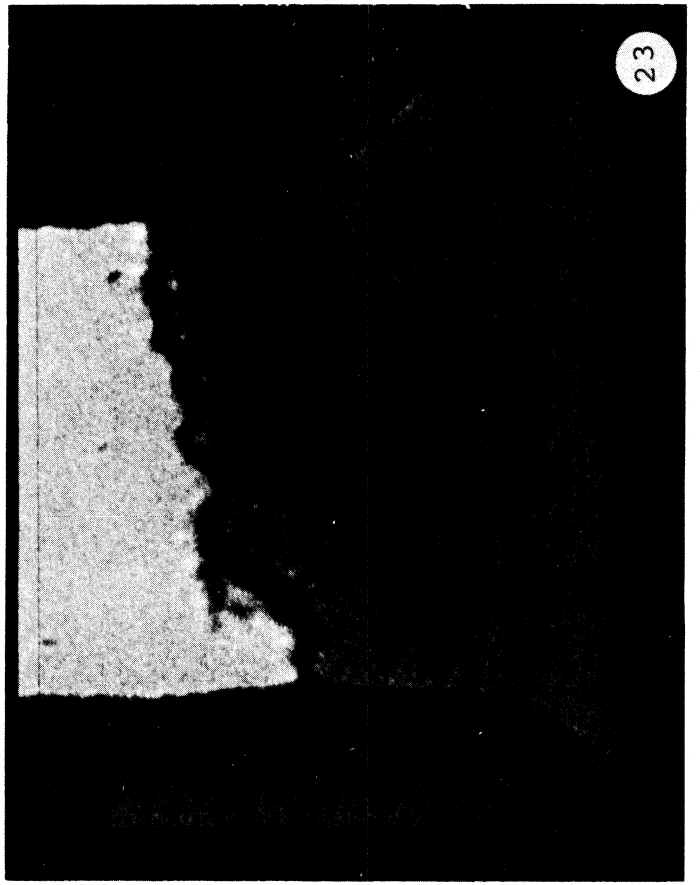


FIGURE 6

SEM PHOTO, (12,000X) USING VOLTAGE CONTRAST OF A NORMALLY FAST BLOWN FUSE WITH A SMALL GAP REGION BUT A HIGH BREAKDOWN STRENGTH ~ 400 VOLTS.

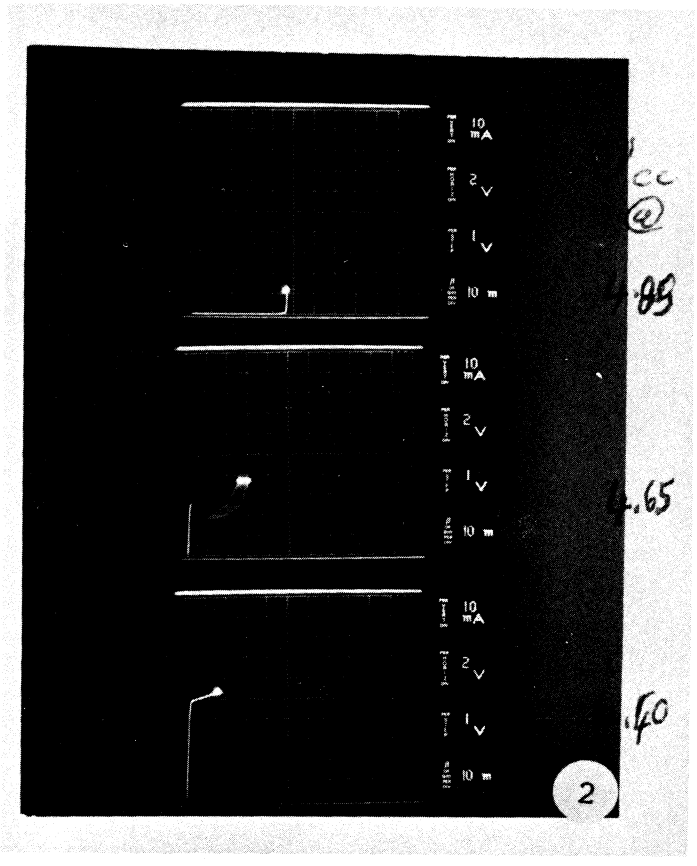


FIGURE 7

V_{OL} /I_{OL} CHARACTERISTIC OF AN OUTPUT HELD AT AN ADDRESS WHERE THE ORIGINALLY PROGRAMMED FUSE "GREW BACK". NOTE THE OUTPUT GOES INTO OSCILLATION AT A V_{CC} OF 4.65 VOLTS AND IS OUT OF SATURATION AT 4.85 VOLTS V_{CC}.

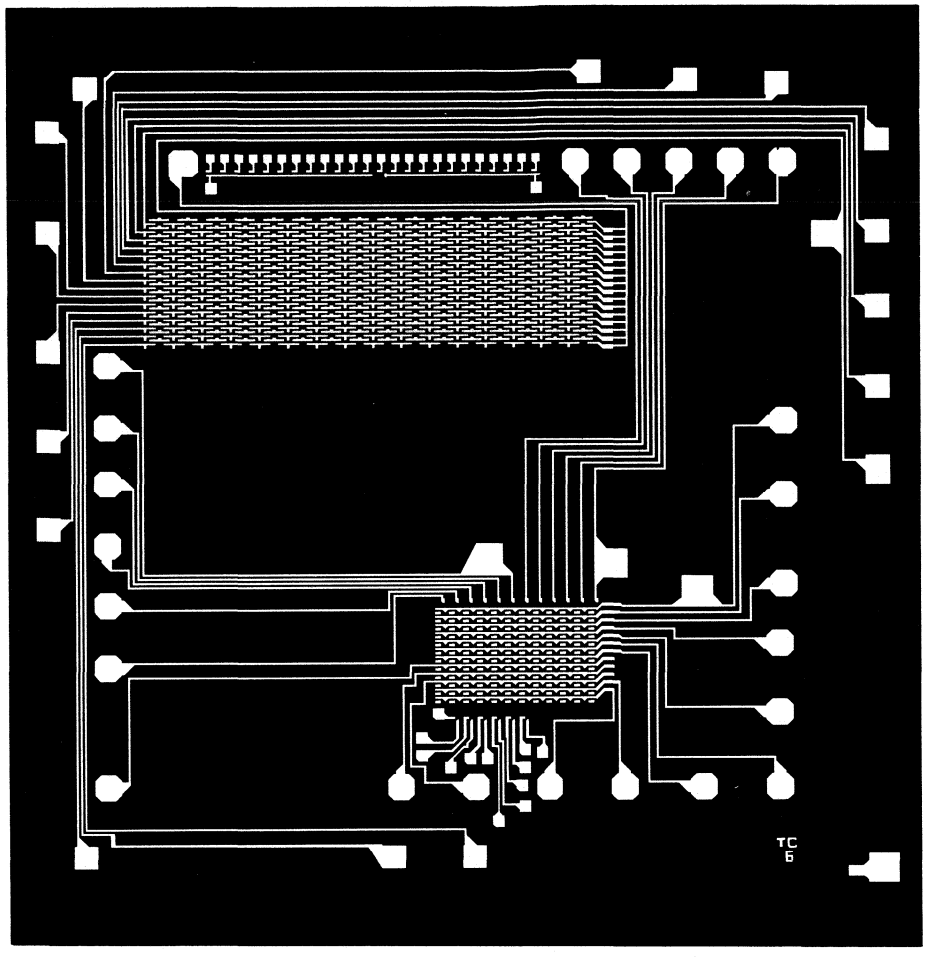


FIGURE 8

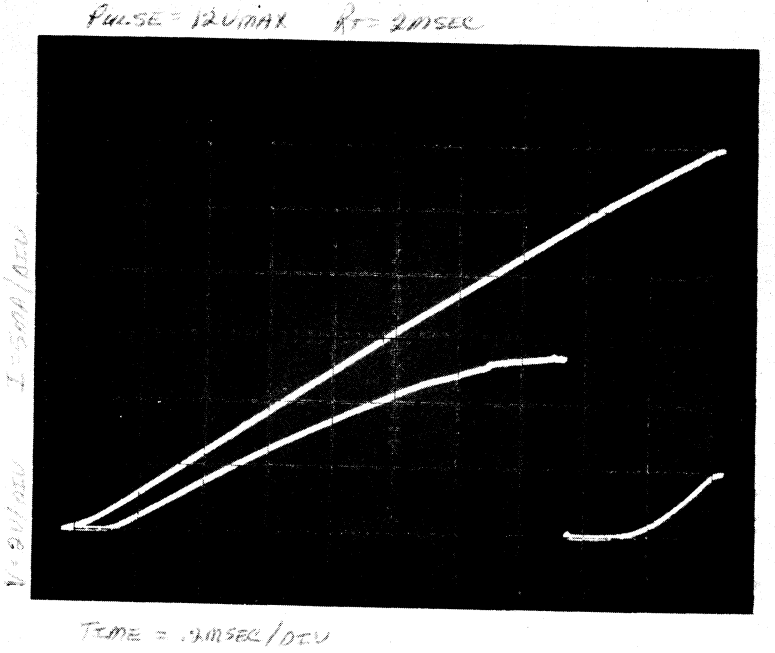


FIGURE 10

FAST PROGRAMMED FUSE STORAGE SCOPE TRACE OF PROGRAMMING CURRENT (BOTTOM) AND PROGRAMMING VOLTAGE (TOP). NOTE ABSENCE OF ANY TRANSITION DURING OPENING OF FUSE.

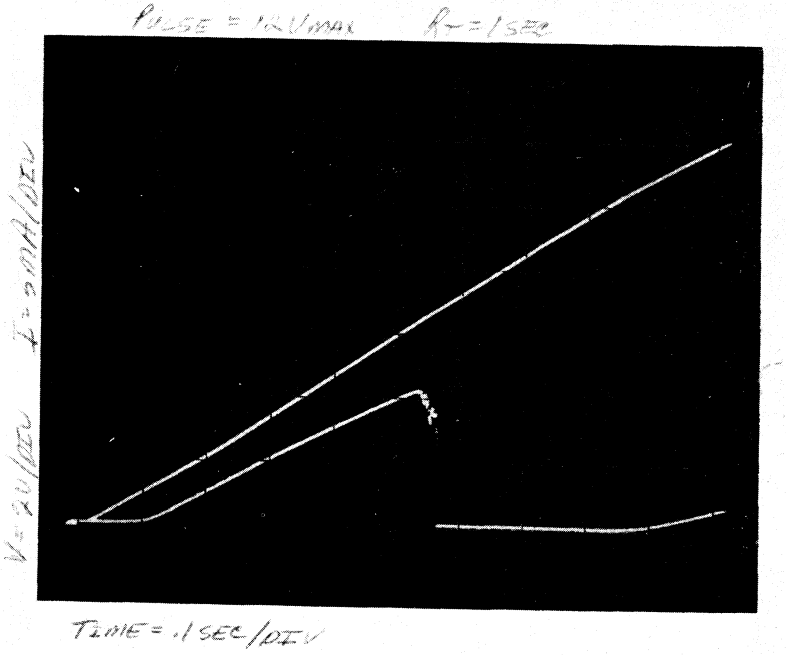


FIGURE 9

SLOWLY PROGRAMMED FUSE: STORAGE SCOPE TRACE OF PROGRAMMING CURRENT (BOTTOM TRACE) AND PROGRAMMING VOLTAGE (TOP TRACE). NOTE UNSTABLE DECAY TRANSITION JUST PRIOR TO OPENING. THIS OPENING MECHANISM TENDS TO PRODUCE FUSES LIKE FIGURE 5B WHICH HAVE A HIGHER PROBABILITY OF "GROW BACK".

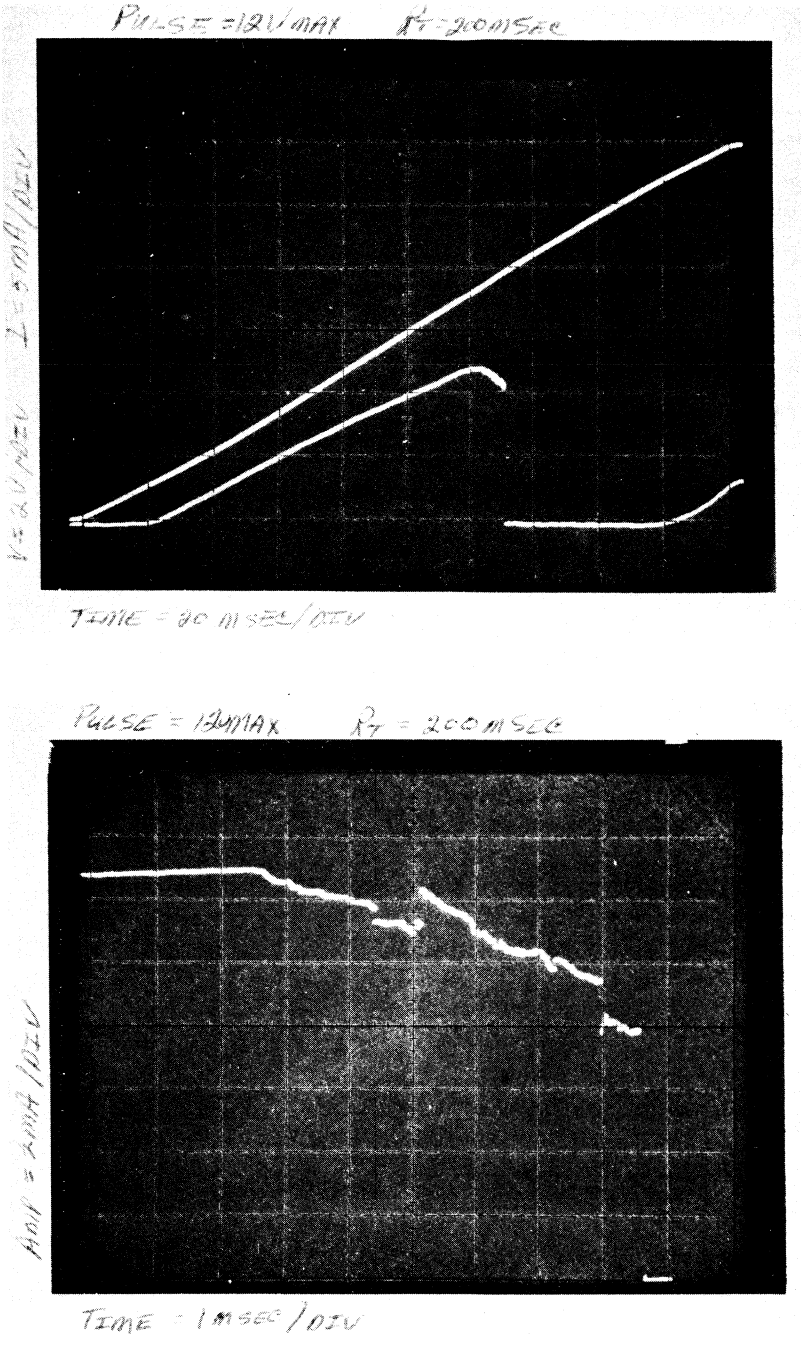


FIGURE 11

BLOW-UP OF THE UNSTABLE INCREASING RESISTANCE REGION JUST PRIOR TO OPENING OF A SLOWLY PROGRAMMED FUSE.

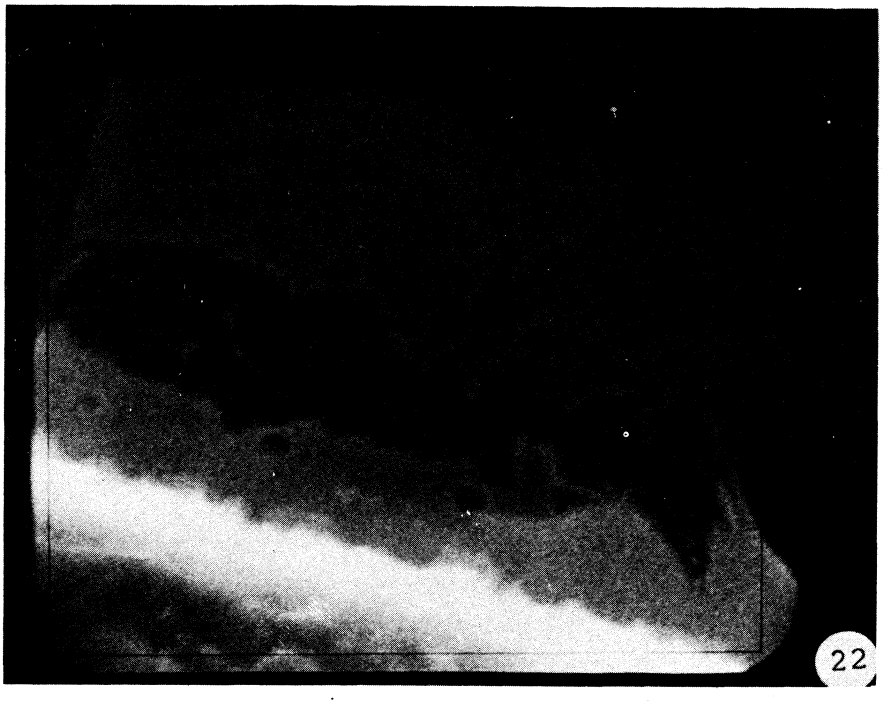
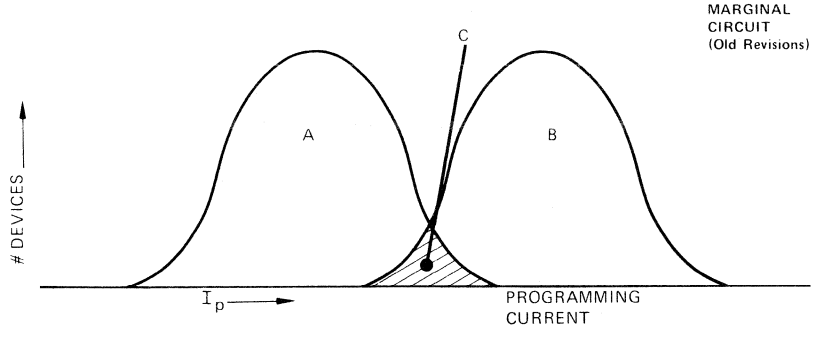


FIGURE 12

SEM PHOTO (20,000X) USING VOLTAGE CONTRAST OF A SLOWLY BLOWN FUSE WITH A LARGE GAP REGION (OPTICALLY) BUT A LOW BREAKDOWN STRENGTH ~ 4 VOLTS. NOTE THE FINGERS AND ISLANDS OF RESIDUAL MATERIAL IN THE GAP. FUSES WITH THESE CHARACTERISTICS HAVE A HIGHER PROBABILITY OF GROW BACK. (SEE FIGURE 6)

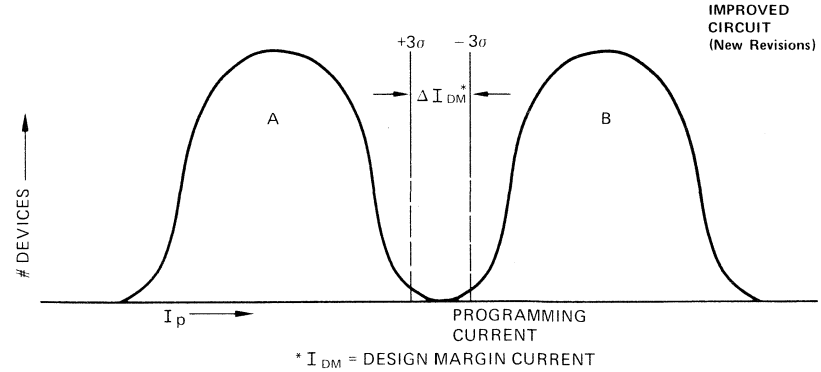
CIRCUIT DESIGN REQUIREMENTS FOR PROGRAMMING CURRENT



A. DISTRIBUTION OF REQUIRED PROGRAMMING CURRENT FOR THE FUSES OVER ALL DEFINED PROCESS VARIATIONS.

B. DISTRIBUTION OF PROGRAMMING CURRENT AVAILABLE TO THE FUSE AND LIMITED BY THE DEVICE CIRCUITRY OVERALL DEFINED PROCESS VARIATIONS.

C. OVERLAP AREA WHERE PROGRAMMING CURRENT IS LIMITED TO THE FUSE PRODUCING FUSES WITH A HIGHER PROBABILITY OF "GROW BACK" AND A NUMBER OF FUSES THAT WON'T PROGRAM.



$^{*}I_{DM}$ = DESIGN MARGIN CURRENT

FIGURE 13

BLOCK DIAGRAM: 256 WORDS x 4 BITS PROGRAMMABLE READ ONLY MEMORY

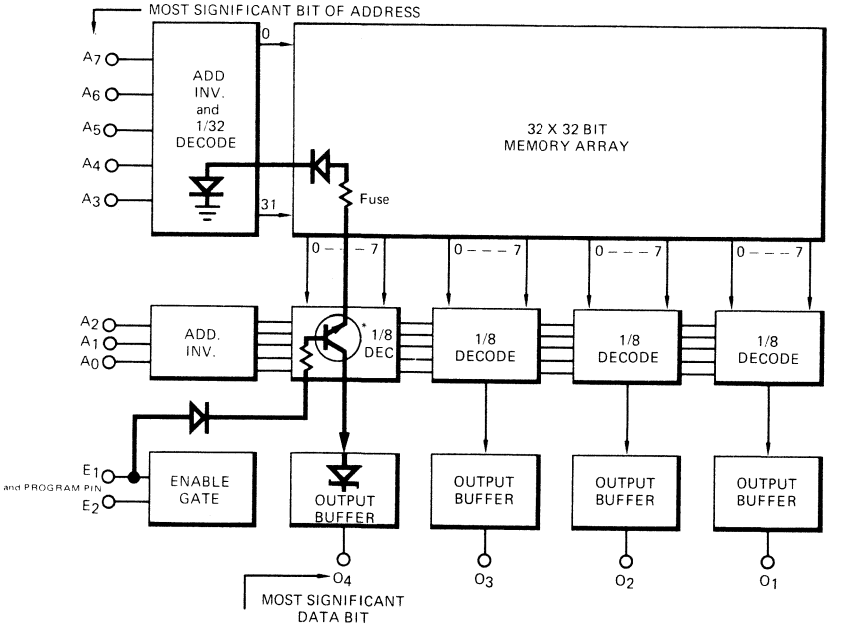
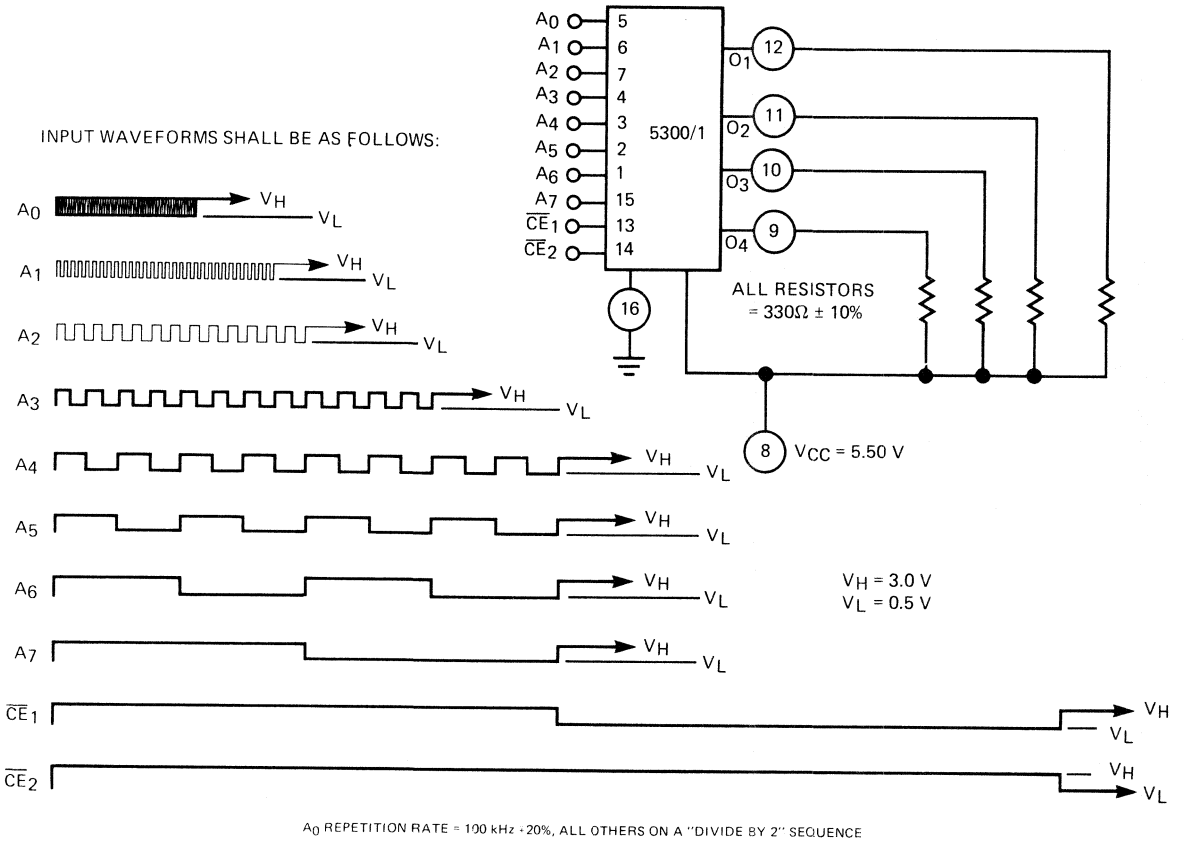


FIGURE 14

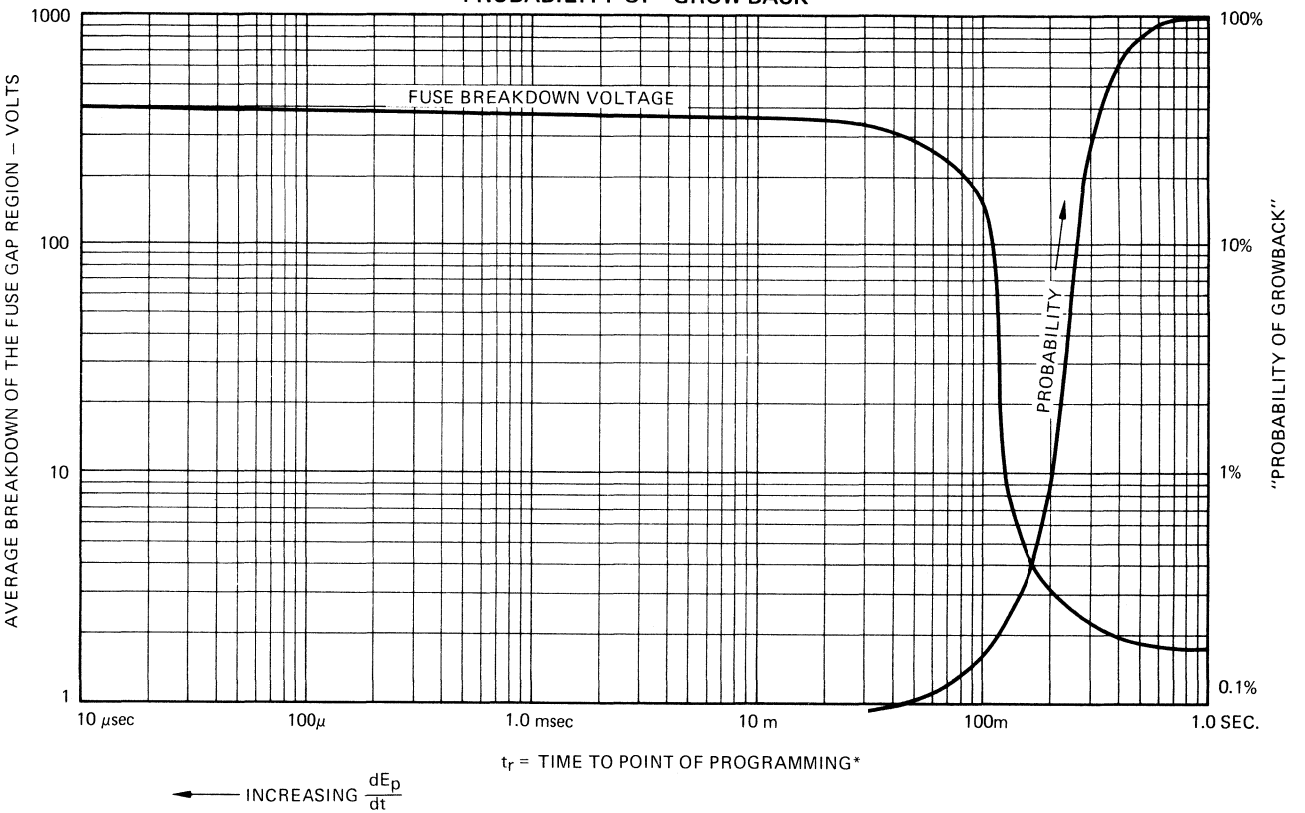


A_0 REPETITION RATE = 100 kHz ±20%, ALL OTHERS ON A "DIVIDE BY 2" SEQUENCE

TYPICAL BURN-IN CIRCUIT MM5300/1

FIGURE 15

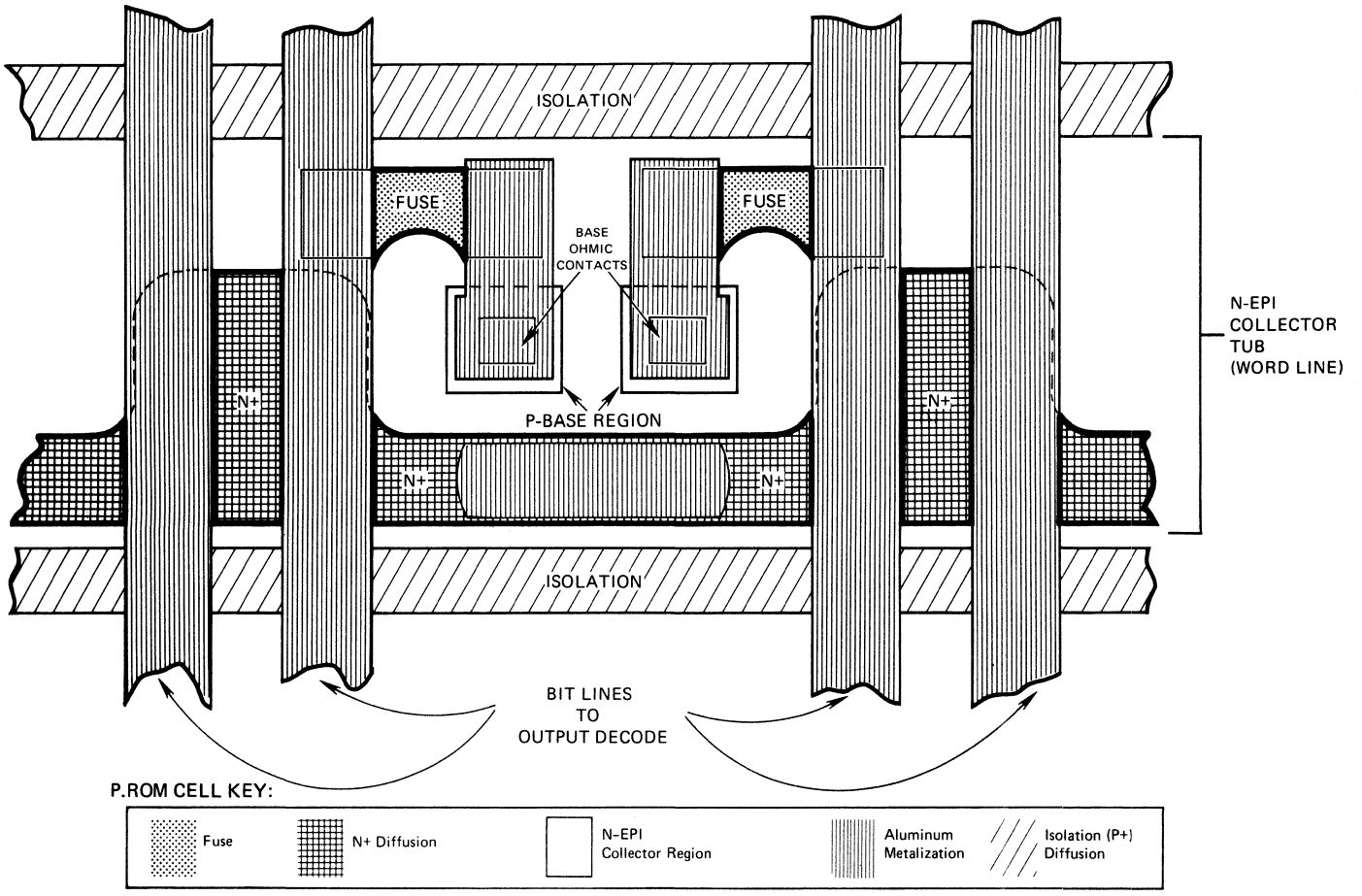
EFFECT OF PROGRAMMING ENERGY, E_p vs. TIME ON FUSE BREAKDOWN VOLTAGE AND PROBABILITY OF "GROW BACK"

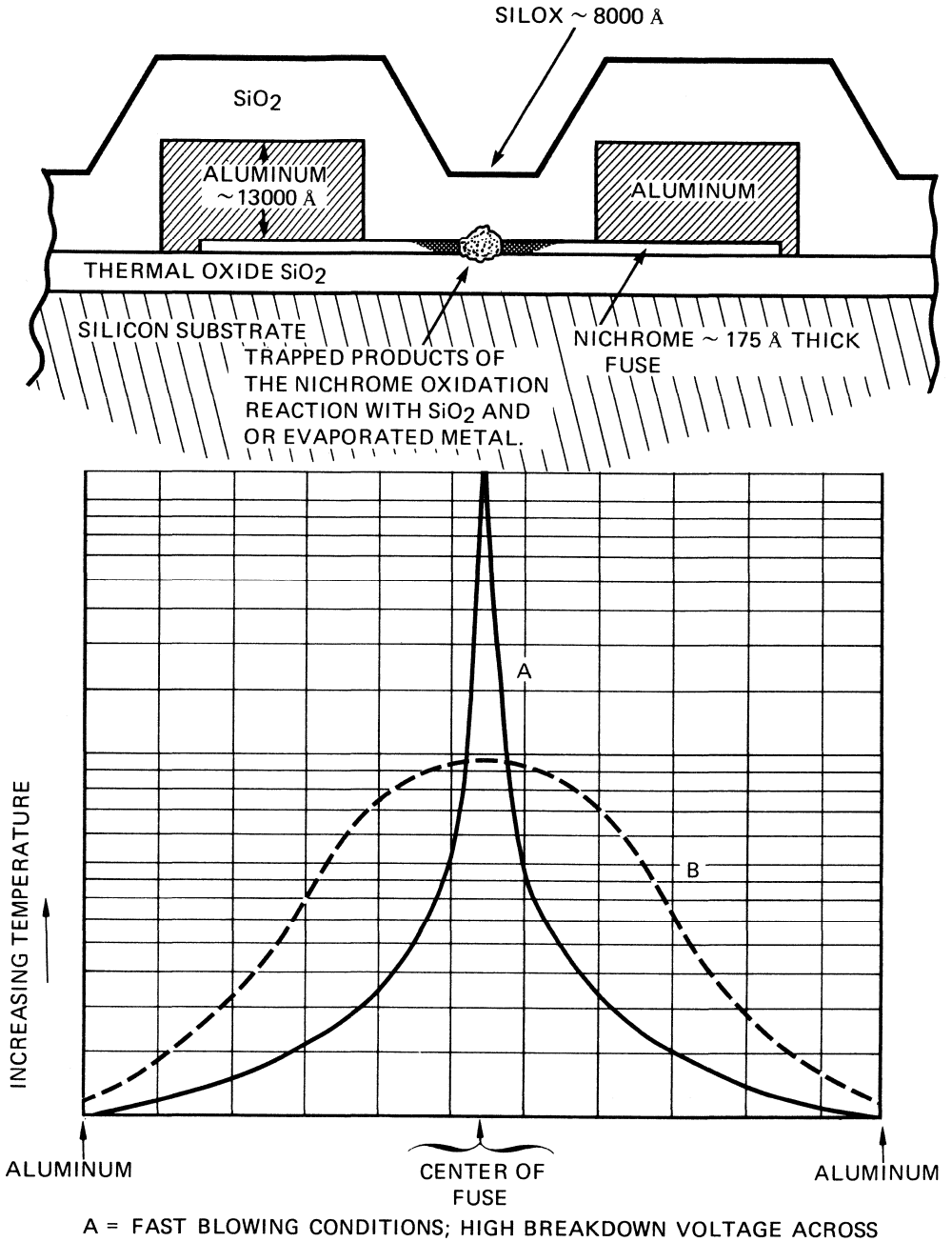


*NOTE: UNLIMITED LINEAR RISE IN VOLTAGE SUCH THAT THE FUSE ALWAYS PROGRAMMED ON THE RISE TIME.

FIGURE 16

TYPICAL P. ROM CELL





A = FAST BLOWING CONDITIONS; HIGH BREAKDOWN VOLTAGE ACROSS GAP RESULTING IN RESISTANCE TO "GROWBACK".

B = SLOW BLOWING CONDITIONS LOW BREAKDOWN VOLTAGE ACROSS GAP RESULTING IN HIGHER PROBABILITY OF "GROWBACK".

FIGURE 18

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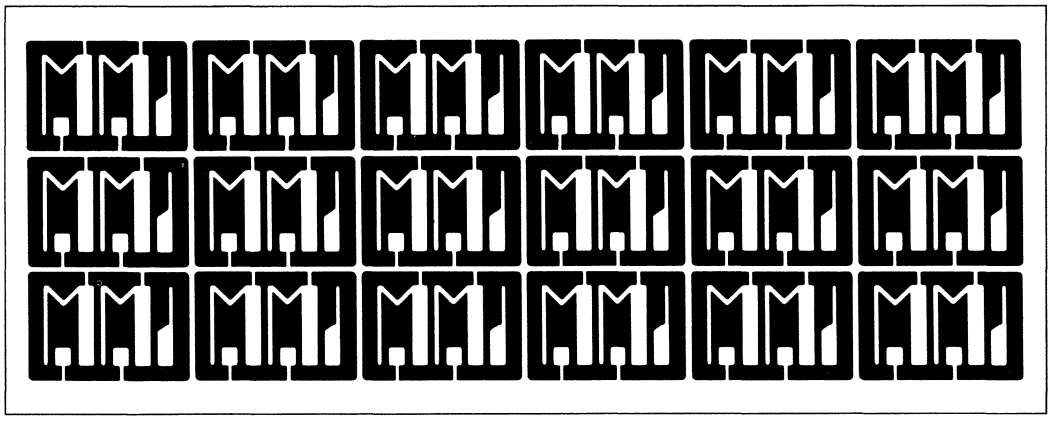
Application Note 110

USE OF BIPOLAR ROM AND P.ROMS



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LARGE BIPOLAR ROMS AND P.ROMS REVOLUTIONIZE CONVENTIONAL LOGIC AND SYSTEM DESIGN

By J. McDowell
Systems & Applications Manager
Monolithic Memories, Inc.

Do you remember when the radicals of a few years ago said that TTL logic would be cheaper than discrete transistors? MMI claims a similar revolution is in the making. "Large ROMs and P.ROMs will replace TTL. In 1975, new designs will not use TTL logic or CMOS logic. ROM controlled (microprogrammed) processors will replace most logic functions."

Let's briefly retrace the steps leading to this "revolution", starting with the terminology we will use.

TERMINOLOGY

A Read Only Memory (ROM) has a fixed data pattern stored in each address location which cannot be readily changed. A typical change might take six (6) weeks and must be made by the semiconductor manufacturer. It is called "read only" to distinguish it from a "read/write" memory where the information can be readily changed.

Programmable Read Only Memories (P.ROMs) are ROMs whose stored data can be readily changed by the user in his facility. The bipolar non-erasable P.ROMs built from nichrome resistors are changed by opening nichrome links and take about 10 seconds to change.

All ROMs and P.ROMs are non-volatile meaning that unlike most semiconductor read/write memories the data is not lost if power goes down.

HISTORY

In 1965 to 1969 engineers argued that there was little need for a ROM since a read/write memory loaded with a suitable pattern could always do the job of a ROM. The argument, at that time, had some merit because most ROMs were built from cores, transformers, capacitors or resistors. Typically, a capacitor or no capacitor, a wired core versus an unwired core, etc., was used to distinguish between a 1 or 0.

These ROMs, at the time, did not look like they could compete with fast 64 bit RAMs of the time and the promises of low cost, high speed read/write memories just around the corner. The ROM advocates, however, realized that they too could use semiconductor technology.

Today, we find semiconductor bipolar ROMs in all sizes and shapes from 256 bits to 10240 bits. The ROMs, at this point in time, are ten (10) times the read/write memory density, 1/5 their cost, and, as a result, have captured a place in the memory hierarchy.

P.ROMs

One of the main drawbacks of the semiconductor ROM was the paper work and the lead time (six to ten weeks) and the $350 to $700 required by the semiconductor manufacturer to make the custom mask required to pick up a diode for a 1 or to leave it unconnected for a zero as required by a particular data pattern.

The P.ROM has eliminated this problem because the user can, in his facility, put a custom code in a P.ROM in a matter of minutes. P.ROM programmers are available which allow manual operation or automatic programming from paper tape, a master device, or a computer. The P.ROMs are pin and performance compatible with their ROM counterparts, offering the user an inexpensive prototyping tool and saving valuable development time. Bipolar P.ROMs are available in all sizes from 256 bits to 4096 bits.

ROM APPLICATIONS—PAST

The growth of the minicomputer industry was a major factor in the growth of semiconductor ROMs. The need for an efficient means of handling the control section of the machine led to the widespread use of microprogramming. Microprogramming uses ROM firmware to replace the conventional logic gates required to execute a machine instruction. For example, ROM outputs can supply the code to control an arithmetic logic unit by having octal coded instruction as the ROM input. Bootstrap loaders, which are required to get the minicomputer on the air and permit the entry of data after a core dump, used to be hand entered—now a ROM is activated. Other users found ROMs efficient as code converters or as trigonometric look up tables.

ROM APPLICATIONS—PRESENT & FUTURE

As larger ROMs become available, it is economical to directly look up many of the arithmetic and logic functions required in a system. The machine tool industry, for example, can program a turret lathe with a ROM look up table to make all the various standard nut and bolt types.

Feeding ROM outputs back as ROM address inputs permits sequential logic to be put in ROMs. Feeding several outputs back as ROM inputs while other outputs are used as controls permits construction of powerful sequence generators, sequence detectors, and hard-wired controllers. An example might be the use of a ROM sequence detector as an automatic takeoff checkout procedure for airplanes or pollution control checkout of automobiles once suitable transducers are developed.

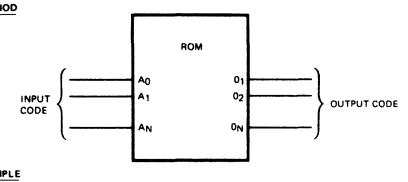
ROMs used in combinatorial logic functions generators can feed ROMs used as counters, or ROMs used as adders, to implement a host of conventional applications. The ROM can also be time shared to perform code conversion at time "A", logic at time "B", and sequence generation at time "C". The applications on the following pages are arranged in order of increasing complexity and should whet your appetite and point the way to a new method of design. All of the applications shown are far more efficient and economical than the conventional TTL implementations. All use parts available *today*.

CODE CONVERTERS

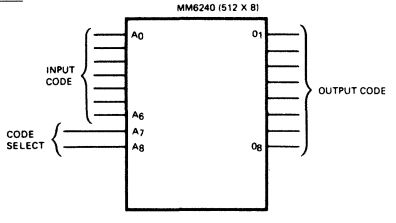
COMMENTS

A 512 word by 8 bit (512 x 8) rom is partitioned into four 128 x 8 sections by addresses A_7 and A_8. A different code converter is mapped into each section. The character fed to the rom address inputs are the input code and the rom is coded with a custom mask to translate each input to a user defined output code.

METHOD



EXAMPLE



INPUT CODE	OUTPUT CODE	ROM REQ'D	CODE SELECT A_8	CODE SELECT A_7
BAUDOT	ASC11	128 X 8	0	0
ASC11-7	EBCIDIC	128 X 8	0	1
SELECTRIC	EBCIDIC	128 X 8	1	0
EBCIDIC	SELECTRIC	128 X 8	1	1

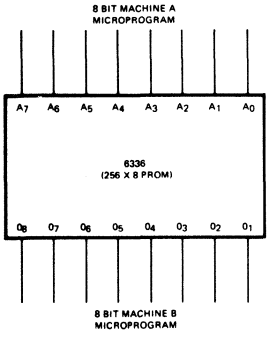
EMULATION

COMMENTS

Most computer manufacturers have made the software of all their machines compatible even though the capabilities and technologies used in the various machines differ widely. The hardware technique for implementing this compatibility is called emulation.

Many transducers or measuring instruments have known and well

EMULATION MEANS MAKING MACHINE B LOOK LIKE MACHINE A BY HAVING MACHINE B USE MACHINE A'S SOFTWARE.



EXAMPLE

THE CODE FOR AN ISZ (INCREMENT AND SKIP IF ZERO) IS $\overset{A_7}{0}\ 1\ 0\ 1\ 0\ 1\ 0\ \overset{A_0}{1}$ IN MACHINE A AND $\overset{O_8}{1}\ 0\ 0\ 1\ 0\ 1\ 1\ \overset{O_1}{0}$ IN MACHINE B MEANING THAT WORD 0 1 0 1 0 1 0 1 OR BINARY 85 SHOULD BE PROGRAMMED WITH 1 0 0 1 0 1 1 0 ON THE PROM OUTPUTS.

TRANSDUCER ERROR CORRECTION

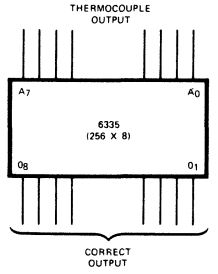
COMMENTS

Many transducers or measuring instruments have known and well defined errors. Correction of these errors is usually impractical because of economic or hardware considerations. Using a rom to improve accuracy in these situations is often quite practical, and can offer dramatic cost/performance improvements. The rom simply looks up the correct value with the incorrect value as its input. Other address lines could be used to position the rom into various ranges where the correction factors may be different.

PROBLEM

A NEWLY DEVELOPED DIGITAL THERMOCOUPLE IS KNOWN TO BE ±4% IN ERROR BETWEEN 55°C AND 0°C, +37% OFF BETWEEN 0°C AND 40°C, AND OBEYS THE EQUATION ERROR (%) = (.25 + TEMPERATURE (.01) .5) BETWEEN 40°C AND 125°C. DEVISE A MEANS OF CORRECTING THE ERROR.

SOLUTION



PROGRAM THE PROM TO CORRECT THE ERROR. FOR EXAMPLE, IF THE THERMOCOUPLE OUTPUT IS 0000100 AND SHOULD BE 0000101 THE ADDRESS INPUT IS BINARY 4 AND THE STORED DATA IS 0000101.

TRIGONOMETRIC LOOK UP TABLES

COMMENTS

In many applications, the speed of the converging series used to generate the trigonometric functions is too slow and the accuracy obtainable by direct look-up requires too much hardware. The availability of 1K x 10 roms extends the direct look-up approach into new areas with a significant reduction in package count and power.

USE A 1024 WORD BY 10 BIT ROM (MM6255) FOR A SIN 0° TO 90° LOOK UP TABLE.

HERE'S HOW

A) INTERPRET THE ROM OUTPUT CODE AS A GROUP OF BINARY WEIGHTED FRACTIONS WHICH MUST BE ADDED FOR THE CORRECT VALUE.

OUTPUT →	O_1	O_2	O_3	- - -	O_{10}
WEIGHT →	1/2	1/4	1/8	- - -	1/1024

B) CONSIDER THE 90° RANGE OF ANGLES TO BE LOCATED IN 1024 WORDS OF ROM ∴ EACH WORD = $\frac{90°}{1024}$ = 088°

EXAMPLE – FIND SIN 71°

A) $\frac{71°}{90°} = \frac{X}{1024\ \text{WORDS}}$

X = WORD 808

B) STORED DATA AT WORD 808 = $\overset{O_1}{1}\ \overset{O_2}{1}\ \overset{O_3}{1}\ \overset{O_4}{1}\ \overset{O_5}{0}\ \overset{O_6}{0}\ \overset{O_7}{1}\ \overset{O_8}{0}\ \overset{O_9}{0}\ \overset{O_{10}}{0}$

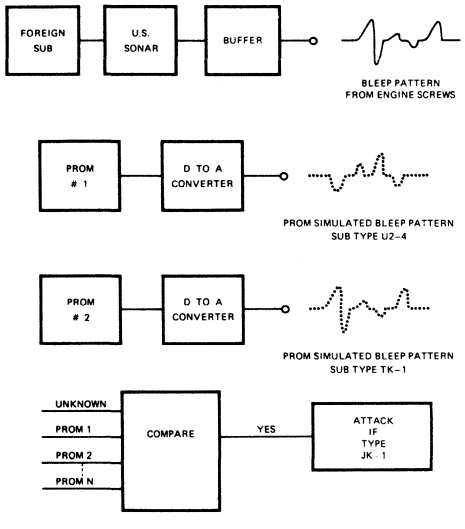
SIN 71° = 94531 = 1/2 + 1/4 + 1/8 + 1/16 + 0 + 0 + 1/128 + 0 + 0 + 0

HANDBOOK VALUE = 94552
OUR VALUE 94531
ERROR 00021 < 1/1024

SUBMARINE IDENTIFIER

COMMENTS

P. roms and roms can be used to generate arbitrary waveforms by counting through the p. rom or rom addresses while the outputs are fed into a digital-to-analog converter. The p. rom or rom is coded to produce the waveforms point by point. Some commercial pulse operations now use these techniques to generate sine, square and triangular waves. Pattern recognition by comparing a known analog signal with an unknown has, as we will see, some interesting possibilities.



METHOD : ENCODE THE PROMS OUTPUT SO THAT EACH INPUT ADDRESS DEFINES ONE POINT ON THE WAVEFORM WHEN ATTACHED TO A D TO A CONVERTER

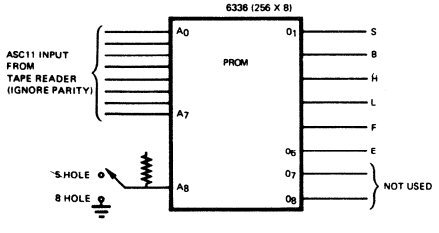
PAPER TAPE INTERPRETER

COMMENTS

Often while designing a system we need to be able to pick out certain combinations of the inputs to give us status or control information. The logic to implement this decoding is usually quite random and consumes significant printed circuit board area. Here is a method to simply decode using roms or p. roms.

PROBLEM

DEVISE A METHOD OF SENSING ASC11 CHARACTERS S, B, H, L, F, AND E IN 5 HOLE AND 8 HOLE TAPE FORMATS FROM A PAPER TAPE READER. THESE DETECTED CHARACTERS WILL INDICATE START, BEGIN, HIGH DATA, LOW DATA, FINISH, AND END TO THE SYSTEM CONTROLLER.



SOLUTION

CONVENTIONAL TTL WOULD REQUIRE A LARGE NUMBER OF GATES TO DECODE THESE CHARACTERS. USING A ROM OR PROM HOWEVER, REDUCES THE PROBLEM TO A SIMPLE CODING OF 12 ADDRESSES (6 FOR 8 HOLE FORMAT AND 6 FOR 5 HOLE FORMAT) SUCH THAT WHEN S FOR EXAMPLE IS DETECTED O_1 AND ONLY O_1 OF THE PROM GOES LOW.

ARITHMETIC FUNCTIONS

COMMENTS

The need to generate special arithmetic functions is often a difficult design problem. Many times the cost of a processor negates its use and yet many processor-like problems must be solved. Using roms for special purpose functions is quite practical where the operands are of small bit length and the output accuracy requirements are not too stringent.

THE FUNCTIONS $F = \sqrt{a^2 + b^2}$ AND $G = \sqrt[3]{a^2 + b^2}$ ARE REQUIRED FOR 4 BIT NUMBERS a AND b. F AND G MUST BE ACCURATE TO ±.09

METHOD

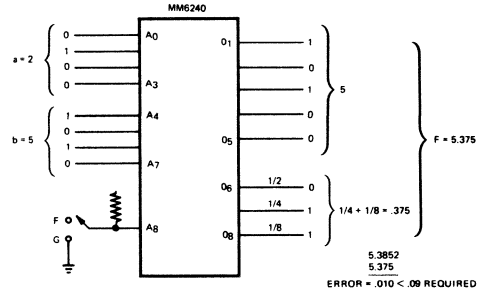
A) LOOK UP ALL POSSIBLE INPUT COMBINATIONS OF a AND b USING 8 ROM ADDRESS INPUTS. USE A 9TH ROM ADDRESS INPUT TO SELECT F OR G.

B) CODE THE FIRST 2^8 WORDS FOR FUNCTION G AND THE LAST 2^8 WORDS FOR F.

C) F WILL BE LARGER THAN G AND HAVE A MAX. VALUE OF 21.21 WHEN a = b = 1111. F MUST THEREFORE BE A 5 BIT BINARY NUMBER (TO REPRESENT THE INTEGER 21). THE ± .09 ACCURACY WILL REQUIRE 3 ROM OUTPUTS WEIGHTED 1/2, 1/4, AND 1/8 WHICH WILL GIVE ACCURACY OF 1/16 OR ±.0625.

EXAMPLE

a = 2, b = 5 $F = \sqrt{2^2 + 5^2} = 5.3852$ (HANDBOOK)

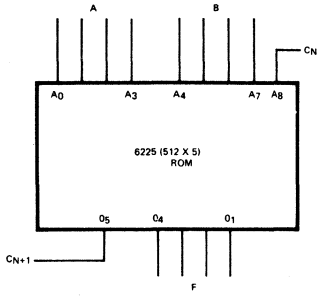


BCD ADDER

COMMENTS

In many inexpensive terminals and calculators, binary arithmetic adds complications and code conversion problems since the readouts must be driven by BCD. A simpler solution is to use BCD throughout. The problem is that conventional adders are binary and require several packages of support circuitry to be able to handle BCD. The large rom offers a simple answer.

DESIGN AN EXPANDABLE BCD ADDER



EXAMPLE

2 = A = 0010
9 = B = 1001
11 = F = 1011

IF C_N=0 THEN 1001 (B) 0010 (A) IS BINARY

ADDRESS 146 WHICH WOULD BE CODED

WITH 1 (C_{N+1}) 0001 (F)

THE SECOND HALF OF THE ROM (WORDS 256 TO 511) WILL BE CODED FOR THE SUM WHEN C_N=1

MULTIPLIER

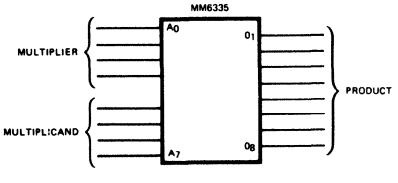
COMMENTS

Many methods of multiplication have been used in computing machines, such as multiple additions, add and shifts, etc. Often a need arises in applications such as Fast Fouries Transforms and Digital Filters for high speed multiplication. The rom offers an attractive solution for sign magnitude multiplication. It simply looks up the required answer like the multiplication tables memorized in grammar school.

4 BIT BY 4 BIT PARALLEL BINARY MULTIPLIER

METHOD

DIRECT LOOK-UP OF PRODUCT



EXAMPLE

MULTIPLIER = 12 = 1100
MULTIPLICAND = 13 = 1101
PRODUCT = 156 = 10011100

8 X 8 MULTIPLIER

DIRECT LOOK-UP REQUIRES 2^{16} X 8 ROM = 512K BITS WHICH IS IMPRACTICAL

METHOD

BREAK 8 X 8 MULTIPLICATION INTO FOUR 4 X 4 MULTIPLICATIONS AND ADD THE RESULTS WITH 2 TTL 4 BIT ADDERS (74S181). THIS REQUIRES ONLY 8K BITS OF ROM.

$$z = x\,y = (a + b)(c + d) = a\,c + b\,c + b\,d$$

x = 8 BIT MULTIPLIER
y = 8 BIT MULTIPLICAND
z = 8 BIT PRODUCT

a = MOST SIG. 4 BITS OF x
b = LEAST SIG. 4 BITS OF x
c = MOST SIG. 4 BITS OF y
d = LEAST SIG. 4 BITS OF y

BINARY DIVIDER (8 BITS ÷ 4 BITS)

COMMENTS

The division of an 8 bit number by a 4 bit number gives a maximum of an 8 bit result (i.e., binary 255 divided by binary 1) and we want ±1/8 accuracy which adds 3 binary digits for a total of an 11 bit quotient. Rather than use a 12 input, 11 output rom (4096 x 11), we can use factoring techniques and adders to significantly reduce the rom or p. rom required. This factoring technique should be considered wherever the large number of rom bits required seems to rule out using roms or p. roms.

METHOD LET X_8 = THE 8 BIT DIVIDEND

Y_4 = THE 4 BIT DIVISOR

F_{11} = THE 11 BIT QUOTIENT (8 BIT RESULT TO ± 1/8 ACCURACY)

$X_8 = B_4 + A_4$

B_4 = MOST SIGNIFICANT FOUR BITS OF X_8

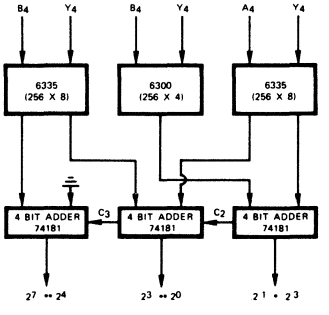
A_4 = LEAST SIGNIFICANT FOUR BITS OF X_8

$$F_{11} = \frac{X_8}{Y_4} = \frac{B_4 + A_4}{Y_4} = \frac{B_4}{Y_4} + \frac{A_4}{Y_4}$$

DIRECT LOOKUP OF $\frac{X_8}{Y_4}$ REQUIRES A 4096 X 11 ROM.

LOOKUP OF $\frac{B_4}{Y_4}$ AND $\frac{A_4}{Y_4}$ REQUIRES LESS THAN 6000 BITS OF ROM AND SEVERAL ADDERS.

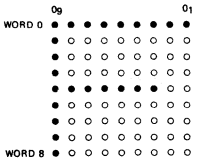
IMPLEMENTATION



CHARACTER GENERATOR

COMMENTS

Most CRT display systems today use roms to generate the required characters. In a 9 by 9 dot font, 9 words of rom are allocated to each character. A row counter would be used to continually count from 0 to 8 to horizontally scan the character. A buffer or shift register memory is normally used to store a line of characters and feeds the character address pins. The parallel load shift register is a parallel to serial converter which feeds the Z axis (intensity control) of a display unit, it will be clocked 9 times the rate of the row counter.

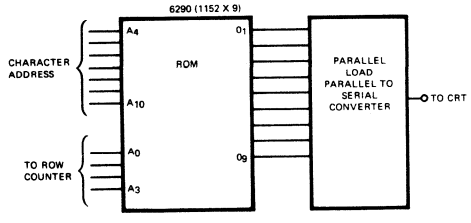


EXPLANATION

THE LETTER "F" IS SHOWN ABOVE FORMED IN A 9 ROW BY 9 COLUMN (9 X 9) FONT OF DOTS. MANY CONVENTIONAL CRT DISPLAYS USE 5 X 7 OR 7 X 9 FONTS THE 9 X 9 FONT GIVES BETTER READABILITY. THE CHARACTERS MAY BE PUT ON THE CRT SEQUENTIALLY ROW BY ROW CALLED ROW SCAN, OR SEQUENTIALLY COLUMN BY COLUMN CALLED COLUMN SCAN.

IMPLEMENTATION

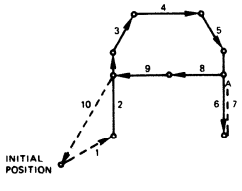
THE FONT IS STORED IN A ROM. IN THE ROW SCAN "F" SHOWN ABOVE 9 WORDS OF A 9 OUTPUT ROM ARE REQUIRED FOR EACH CHARACTER. THE 6290 AN 1152 X 9 ROM STORES THE ENTIRE SET OF 128 ASC11 CHARACTERS IN A 9 X 9 FONT.



VECTOR GENERATOR

COMMENTS

Are you tired of hard to read character fonts made from dot matrices? Try vector generators and design your own characters with the strokes you learned in school. The technique is also applicable to such diverse applications as terrain maps, blueprints and fixed pattern displays.

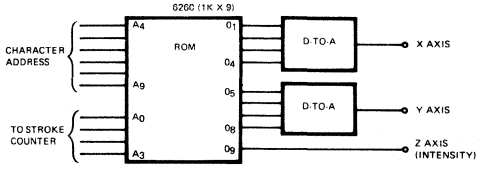


EXPLANATION

THE LETTER "A" SHOWN ABOVE IS FORMED BY A SERIES OF STROKES NUMBERED 1 THRU 10. THE DASHED LINES INDICATE THAT THE CRT BEAM IS BLANKED OFF. THIS METHOD OF CHARACTER GENERATION GREATLY IMPROVES THE RESOLUTION OF A DISPLAY WHEN COMPARED TO CONVENTIONAL DOT MATRIX FONTS. THE 1K X 9 ROM BELOW STORES 102 CHARACTERS.

METHOD

EACH CHARACTER BEGINS AT THE INITIAL POSITION SHOWN ABOVE. RATHER THAN GENERATING THE ABSOLUTE COORDINATES OF X AND Y ONLY CHANGES IN COORDINATE LOCATIONS ARE GENERATED AT PROPER STROKE TIME. ANOTHER ROM BIT DECIDES WHETHER THE STROKE IS BLANKED OR UNBLANKED.



RANDOM LOGIC REPLACEMENT

COMMENTS

Never again should TTL be thought of when random logic functions are encountered. TTL should be the last resort--not the first and final implementation considered. Burn all your college textbooks on Karnaugh maps, minimization theory, etc.; p. roms are the only way to go. P. roms are literally universal logic blocks.

IMPLEMENT THE FOLLOWING EQUATIONS:

$F_1 = (\overline{A}\,B\,C\,D + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,D + A\,B\,C\,\overline{D}) \cdot \overline{E}\,\overline{F}\,\overline{G}\,\overline{H}$

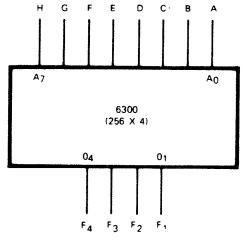
$F_2 = (\overline{A}\,\overline{B}\,C\,D + B\,C\,\overline{D}) \cdot E\,F\,G\,H$

$F_3 = A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,\overline{D} + E\,\overline{F}\,\overline{G}\,H$

$F_4 = A\,B\,C\,\overline{D} \oplus \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} \oplus C\,D\,E$

HERE'S HOW

CODE THE PROM WORD WHERE THE EQUATION IS TRUE WITH A 1 AND LEAVE ALL OTHER LOCATIONS 0



EXAMPLE

F_1 IS HIGH IF ADDRESS 14, 13, 11 OR 7 IS SELECTED AS CAN BE SEEN FROM THE EQUATION ABOVE. IF A IS ASSIGNED WEIGH 2^0, B IS 2^1, ETC. THEN $\overline{A}\,B\,C\,D$ = WORD 14 AND $A\,\overline{B}\,C\,D$ = WORD 13, ETC.

THE PROM REPLACES AT LEAST 12 TTL PACKAGES

HOW MANY BITS OF ROM DOES IT TAKE TO REPLACE A TTL GATE?

COMMENTS

The question of how many bits of rom are equivalent to a gate is frequently asked. No substantiated data has, as far as we know, been published. We have randomly chosen some TTL part numbers and used the published number of gates used in the particular part type's advertisement to attempt to answer the question. The results indicate that large roms can be extremely cost effective.

RANDOM SAMPLE		TTL PACKAGE CHARACTERISTICS			ROM CHARACTERISTICS	
TTL TYPE	FUNCTION	NUMBER OF GATES	NUMBER OF INPUTS	NUMBER OF OUTPUTS	ROM REQ'D	BITS OF ROM PER GATE
7404	HEX INVERTER	6	6	6	64 X 6	$\frac{64 \times 6}{6} = 64$
74180	PARITY GENERATOR	27	9	2	512 X 2	36
7442	BCD TO DECIMAL	18	4	10	16 X 10	9
7443	EXCESS 3 TO DECIMAL	18	4	10	16 X 10	9
7447	BCD TO 7 SEGMENT	34	5	7	32 X 7	7
74155	2 TO 4 DECODE	15	6	2	64 X 2	8
7482	2 BIT ADDER	21	5	3	32 X 3	4
7400	QUAD NAND GATE	4	8	4	256 X 4	256
7486	QUAD EXCLUSIVE OR	8	8	4	256 X 4	128
7483	4 BIT ADDER	42	9	5	512 X 5	61
74151	8 TO 1 SELECTOR	17	11	2	2 K X 2	235
7451	AND OR INVERT	6	8	2	256 X 2	85
74181	ARITHMETIC LOGIC UNIT	75	14	8	16 K X 8	2000

CONCLUSION

THERE IS NO SIMPLE ANSWER, BUT IF WE ELIMINATE THE 74151 AND 74181 ABOVE, THE TOTAL ROM REQUIRED IS 7288 BITS TO REPLACE 199 GATES OR AN AVERAGE OF 37 BITS OF ROM PER GATE. IF WE REPLACE THE 199 GATES WITH ONE 8192 BIT ROM (6280), WE WILL SAVE 10 PACKAGES, 109 INPUTS AND OUTPUTS AND 1.4 WATTS. WE HAVE HOWEVER, ASSUMED THAT ALL REPLACED FUNCTIONS ARE NOT REQUIRED AT ONCE AND THAT THE ROM SPEED IS ADEQUATE.

ECONOMICS OF LOGIC REPLACEMENT

COMMENTS

Manufacturers have found a wide difference between the component cost of a TTL gate and the cost when it is put on a board and the labor and overhead are added. We have tabulated typical costs and show that the average cost of a gate when put on a board and tested is 30¢, whereas the cost of the component is 6¢. Using the cost per gate and knowing the number of rom bits to replace a gate, we can study the economics of replacing logic with roms.

SYSTEM COST OF A 16 PIN DIP ON A 90 PIN 75 IC BOARD

I.C. (4 GATES/PKG)	$ .25
P.C. CARD	.27
INCOMING INSPECTION	.07
COMPONENT INSERTION	.05
BOARD DEBUG	.18
CONNECTORS	.05
CAPACITORS	.04
WIRING	.12
POWER SUPPLY @ $1.00/WATT	.05
CABINETRY/FANS	.17
	$1.20

AVG COST/GATE = 1.20/4 = 30¢ WHEN PUT ON A BOARD.

ASSUMING 36 BITS OF ROM PER GATE AS CALCULATED IN THE PREVIOUS EXAMPLE, AND $.35/BIT FOR THE COST OF A 1 K X 10 ROM (6255), WE CAN CALCULATE THE FOLLOWING SAVINGS:

10 K ROM COST @ $.35/BIT	$ 30.72
NO. OF GATES REPLACED (10240/36)	284. GATES
VALUE OF GATES REPLACED @ $.30/GATE	85.20
$ SAVED PER 10 K ROM USED	$ 54.48
POWER SAVED @ 10 mW/GATE	2.70 WATTS
BOARD AREA SAVED AT 1 IN^2/PKG	70.00 IN^2

VOICE SYNTHESIZER

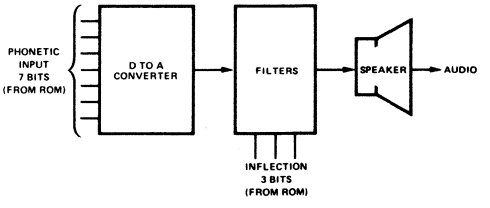
COMMENTS

The synthesis of the human voice is feasible and there are several machines now available which emit sentences which are indistinguishable from the human voice. Several of these machines use a rom to store the vocabulary. Relatively large vocabularies can be constructed with a few rom packages. The digital inputs of the rom permit the synthesizer to be driven by a computer which assembles the required phrases or from another rom in the case of fixed messages.

ANY WORD IN ANY LANGUAGE CAN BE SYNTHESIZED BY AN APPROPRIATE SEQUENCE OF PHONEME COMMANDS. EACH PHONEME COMMAND CONSISTS OF A PARALLEL 10 BIT BINARY WORD. WE WILL ASSIGN 7 BITS TO THE CHOICE OF PHONETIC INPUTS AND 3 BITS TO THE INFLECTION. THERE ARE ROUGHLY AS MANY PHONEMES IN A WORD AS THERE ARE LETTERS. FOR EXAMPLE, THE WORD "HELLO" WRITTEN PHONETICALLY BECOMES HELUŌ AND REQUIRES 5 PHONEMES AT 10 BINARY BITS PER PHONEME.

AN AVERAGE VOCABULARY WILL REQUIRE 6 PHONEMES PER WORD. THEREFORE A 170 WORD VOCABULARY CAN BE PUT IN A 1024 WORD BY 10 BIT ROM (6255)

IMPLEMENTATION

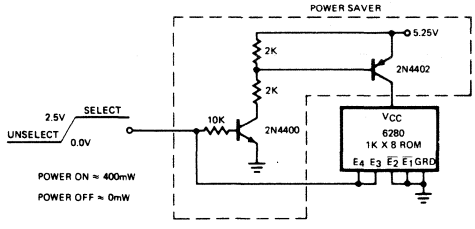


POWER SAVER

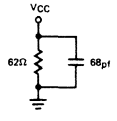
COMMENTS

In airborne systems and in other applications, low power is an absolute necessity. The power saver circuitry shown turns off the Vcc of the rom when it is not in use so that it and the power control circuitry dissipate no power when the device is not being used. Since the rom is a non-volatile, hard-wired storage, it does not lose data if power is removed.

THE POWER SAVER CIRCUIT SHOWN BELOW SWITCHES THE MEMORY V_{CC} ON ONLY WHEN THE PACKAGE IS SELECTED.



THE 6280 EQUIVALENT CIRCUIT FOR CALCULATING THE CAPACITANCE AND CURRENT WHICH MUST BE DRIVEN IS APPROXIMATELY



IN AN ARRAY OF 6280'S SUCH AS A 8K X 72 ROM SYSTEM, THE POWER SAVER CIRCUIT WOULD POWER UP 9 PACKAGES OUT OF THE 72 PACKAGES REQUIRED SAVING ABOUT 29 WATTS.

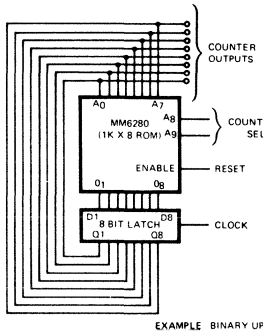
SEQUENTIAL LOGIC REPLACEMENT

COMMENTS

Roms can be used to replace most sequential logic functions if rom outputs are tied back as rom inputs. A latch on the rom outputs is required to avoid the race condition associated with outputs of varying speed tied back to inputs of varying speed. The main advantage of roms is the simplicity with which relatively complex sequences can be generated and the reduced parts count required.

BUILD THE FOLLOWING SYNCHRONOUS 8 BIT COUNTERS
BINARY UP, BINARY DOWN, BCD UP, GRAY CODE

HERE'S HOW



A_8	A_9	ROM WORDS	COUNTER TYPE
0	0	0 TO 255	BINARY UP
0	1	256 TO 511	BINARY DOWN
1	0	512 TO 767	BCD UP
1	1	768 TO 1023	GRAY CODE

EXAMPLE BINARY UP

WORDS	OUTPUT (BINARY)
0	1
1	2
2	3
⋮	⋮
255	0

AN 8 BIT COUNTER REQUIRES AN 8 OUTPUT ROM. ASSIGN 256 ROM WORDS TO EACH COUNTER TYPE. USE THE ROM ENABLE AS A COUNTER RESET. WHEN THE ENABLE IS HIGH THE ROM OUTPUTS ARE HIGH, SO THAT AFTER THE NEXT CLOCK PULSE THE LAST ADDRESS IN THE SELECTED BLOCK OF 256 WORDS WILL BEGIN THE SEQUENCE.

MICROPROGRAMMED TIMING GENERATOR

COMMENTS

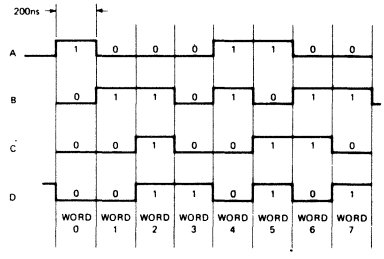
The generation of system timings usually employs counter, decoders and JK flip-flops to get the control pulses required. The rom or p.rom, however, offers a novel way of generating pulse trains. If a mistake is made using logic to generate the pulses, board rework is required. With p.roms, however, another unit can be programmed to correct the error with no board modifications.

PROBLEM

A MINICOMPUTER HAS 32 MEMORY REFERENCE INSTRUCTIONS, EACH OF WHICH HAS DIFFERENT TIMING REQUIREMENTS ON SIGNAL LINES A THRU D. DESIGN A VERSATILE TIMING GENERATOR BASED ON A 200ns CLOCK. ALL INSTRUCTIONS REQUIRE 8 CLOCK CYCLES.

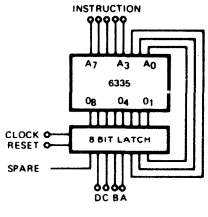
EXAMPLE

A JUMP (JMP) INSTRUCTION REQUIRES THE FOLLOWING PULSES ON A THRU D.



SOLUTION

USE A 256 X 8 PROM WITH 3 OUTPUTS FED BACK TO INPUTS TO MAKE AN 8 STAGE COUNTER FOR THE 8 CLOCK CYCLES REQUIRED FOR EACH INSTRUCTION CODE. EACH ROM WORD WITH THE OUTPUT PATTERN REQUIRED ON ABCD. FOR EXAMPLE WORD 0 AS SHOWN MUST HAVE 1000. 32 DIFFERENT 8 COUNT SEQUENCES ON 4 LINES ARE GENERATED BY THE CIRCUITRY ON THE RIGHT



MICROPROGRAMMING

COMMENTS

The possibility of using roms to implement the control section of a computer was first suggested by M. V. Wilkes in 1951. The concept was first used by IBM in the System 360 Computer. The advantage of the rom is that the hardwired decoders and multiplexers and random logic usually used to implement the control section are eliminated. The rom or p. rom contents personalize the machine and permit changes without new printed circuit boards. The disadvantages of the microprogrammed machine are the difficulties in getting the rom contents debugged. P. roms have helped solve this objection and as a result today, most new minicomputers and processors are microprogrammed.

DESIGN CONTROL CIRCUITRY WHICH WILL PERMIT ANY OF 4 PERIPHERALS TO APPEAR AT THE "A" PORT OF AN ARITHMETIC LOGIC UNIT (ALU) AND ALLOW EITHER THE STORAGE DATA REGISTER (SDR) OR THE PROGRAM COUNTER (PC) INTO THE "B" PORT OF THE ALU.

THE ALU MUST BE ABLE TO INCREMENT, DECREMENT OR TRANSFER THE "A" OR "B" PORT TO THE OUTPUT "F" AS WELL AS ADDITION AND SUBTRACTION OF THE "A" AND "B" PORTS.

ALU

S_2	S_1	S_0	MODE
0	0	0	INCREMENT
0	0	1	DECREMENT
0	1	0	TRANSFER
0	1	1	ADD
1	0	0	SUBTRACT

0/1 TRUE/COMPL

S_7	S_6	MODE
0	0	FORCE 0
0	1	FORCE 1
1	0	TRUE
1	1	COMPL

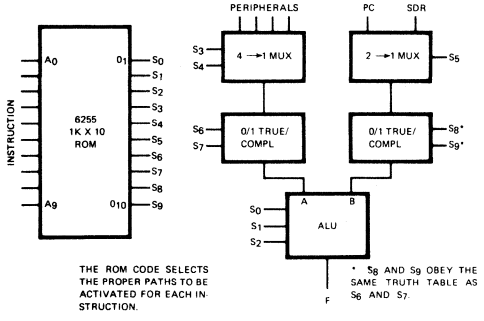
4 ⟶ 1 MUX

S_4	S_3	MODE
0	0	TAPE
0	1	DISC
1	0	CASSETTE
1	1	CORE

2 ⟶ 1 MUX

S_5	MODE
0	SDR
1	PC

IMPLEMENTATION



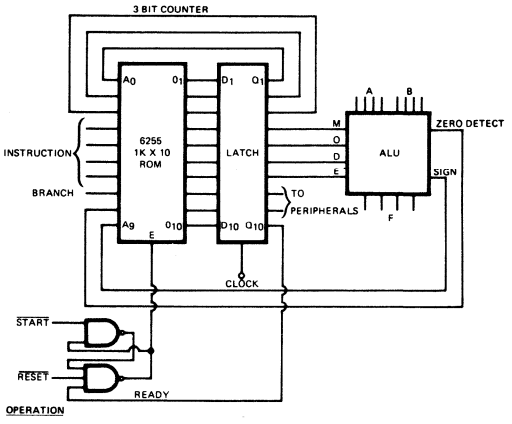
THE ROM CODE SELECTS THE PROPER PATHS TO BE ACTIVATED FOR EACH INSTRUCTION.

* S_8 AND S_9 OBEY THE SAME TRUTH TABLE AS S_6 AND S_7.

HARDWIRED CONTROLLER

COMMENTS

The rapid development of microprocessors in the last two years has left many design engineers in a state of "future shock." Similar developments have taken place in the less publicized field of dedicated hardwired controllers. In many applications, a sequence of unchangeable operations must be executed as a function of switches, levers, relays, etc. Hardwired controllers which are sub-microprocessors in complexity are perfect for these applications.



OPERATION

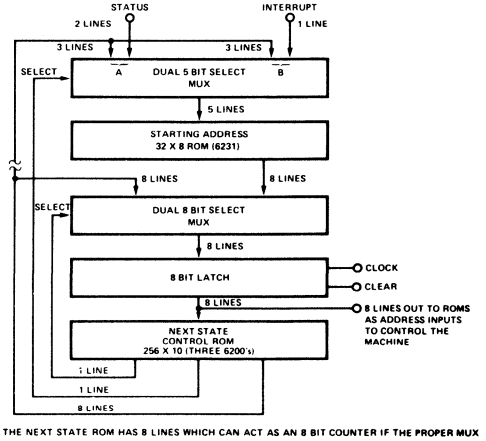
THE NAND GATE LATCH IS USED TO DEFINE A KNOWN STARTING ADDRESS FOR THE ROM. WHEN THE ENABLE (E) IS HIGH THE ROM OUTPUTS ARE HIGH DEFINING A STARTING ADDRESS. THREE ROM OUTPUTS FORM A 3 BIT COUNTER, 4 ARE USED TO CONTROL THE ALU, 2 ARE USED FOR PERIPHERALS AND 1 INDICATES READY. THE ROM STORES 128 DIFFERENT 8 COUNT SEQUENCES WHICH ARE SELECTED BY THE INSTRUCTION, BRANCH AND ALU SIGN AND ZERO DETECTOR.

SEQUENCE CONTROLLER

COMMENTS

Most microprogrammed systems use roms in a sequence control application. Rom outputs are fed back as rom inputs through multiplexers and some rom outputs in addition control the next state. Some people use a starting address rom which decodes the operation code of a computer and points to an address in another rom which might execute 10 micro-operations to emulate an operation and then let in the next operation code using the sequence controller arrangement shown.

DESIGN A CONTROLLER THAT HAS 32 DIFFERENT SEQUENCES ON 8 OUTPUT LINES, 2 TO 255 STEPS LONG. THE SEQUENCES MUST BE CAPABLE OF A 4 WAY BRANCH BASED ON THE STATUS FLAGS AND A ONE WAY BRANCH BASED ON THE INTERRUPT FLAG.



THE NEXT STATE ROM HAS 8 LINES WHICH CAN ACT AS AN 8 BIT COUNTER IF THE PROPER MUX PATHS ARE ACTIVATED. IT CAN ALSO ALLOW THE STARTING ADDRESS ROM TO BE ITS NEXT STATE. TWO STATUS LINES PERMIT CHOICE OF 4 POSSIBLE STARTING ADDRESSES PROVIDING 4 WAY BRANCHING. INTERRUPT IN LIKE MANNER PROVIDES 2 WAY BRANCHING.

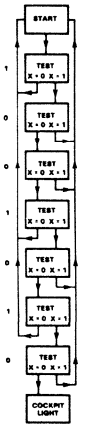
SERIAL CODE DETECTOR OR LOCK

COMMENTS

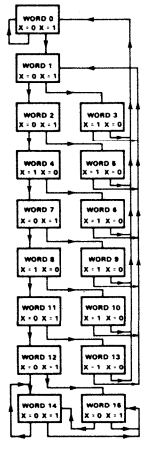
Serial operation can greatly simplify the electonics in many systems where speed is not an overriding concern. Serial operation, however, often complicates system control characters' detection since they must be converted to parallel and then decoded to decide what to do next. Using rom or p. roms as shown here, we can detect sequences with a small amount of hardware.

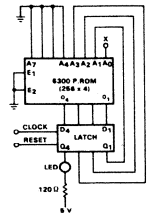
A TRANSDUCER IN AN AIRPLANE SENDS THE SEQUENCE 1001010 IN SERIAL OVER A SINGLE WIRE BUS WHEN THE LANDING WHEELS ARE DOWN. DETECT THIS SEQUENCE CALLED X AND LIGHT A LIGHT IN THE COCKPIT. HOLD THE LIGHT ON UNTIL A RESET IS APPLIED.

FLOW CHART



POSSIBLE SOLUTION
1 = TTL HIGH





REQUIRED PROGRAMMING

WORD	DATA O_4 O_1
0	1 0 0 0
1	1 0 0 1
2	1 0 1 0
3	1 0 0 0
4	1 0 1 1
5	1 0 0 0
6	1 0 0 0
7	1 1 0 0
8	1 1 0 1
9	1 0 0 0
10	1 0 0 0
11	1 1 1 0
12	0 1 1 1
13	1 0 0 0
14	0 1 1 1
15	0 1 1 1

Note that X is tied to A_0 so each branch decision chooses an even or odd address as required.

COMBINATION LOCK

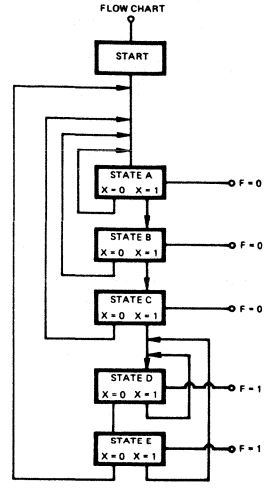
COMMENTS

Most logic designers at one time or another have studied sequential logic, Karnaugh maps, and state assignments. Given a sequential logic problem, the designer usually thinks of JK flip-flops and combinational logic to determine the next state as a function of the present state and input conditions. The assignment of states to minimize hardware is a trial and error procedure since many of the approaches required have not yet been developed in logic theory. Using p. roms and roms and a flow chart, however, the problem can be solved simply in a matter of minutes.

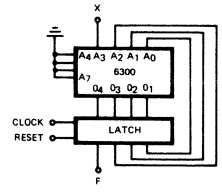
DESIGN A CIRCUIT WHICH AFTER INITIALLY SET TO ZERO, WILL GO TO 1 IF 3 OR MORE CONSECUTIVE 1'S APPEAR ON THE INPUT. IT SHOULD REMAIN AT LOGICAL 1 UNTIL TWO CONSECUTIVE LOGICAL 0'S APPEAR. ASSUME A "1" IS A TTL HIGH LEVEL. ASSIGN MACHINE STATES A THRU E TO THE FIVE POSSIBLE STATES OF THE SYSTEM AND CALL THE OUTPUT F AND THE INPUT X.

PRESENT STATE	NEXT STATE X = 0	NEXT STATE X = 1	OUTPUT F OF PRESENT STATE
A	A	B	0
B	A	C	0
C	A	D	0
D	E	D	1
E	A	D	1

FLOW CHART



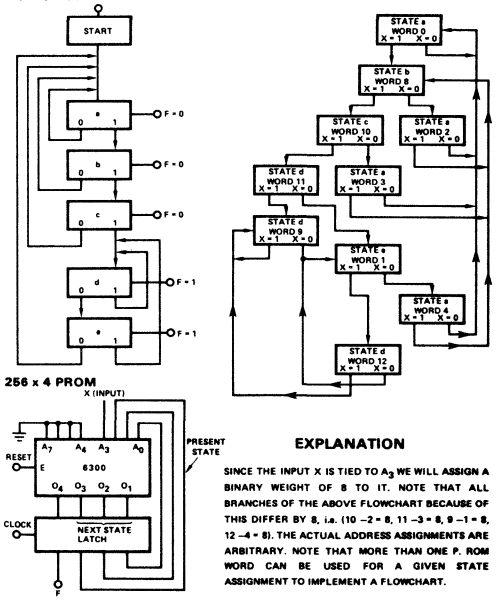
SOLUTION USE A 256 X 4 PROM



BINARY WORD	DATA O_4 O_1	STATE
0	0000	A
1	1100	E
2	0000	A
3	0000	A
4	0000	A
8	0010	B
9	1001	D
10	0011	C
11	1001	D
12	1001	D

THIS SOLUTION IS NOT UNIQUE. NOTE THAT MORE THAN ONE ROM WORD MAY BE ASSIGNED TO A STATE TO IMPLEMENT THE REQUIRED BRANCHING.

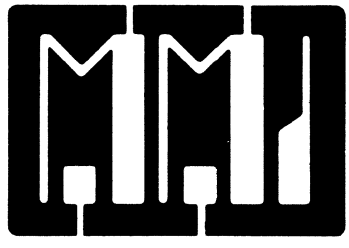
FLOW CHART



256 x 4 PROM

EXPLANATION

SINCE THE INPUT X IS TIED TO A_3 WE WILL ASSIGN A BINARY WEIGHT OF 8 TO IT. NOTE THAT ALL BRANCHES OF THE ABOVE FLOWCHART BECAUSE OF THIS DIFFER BY 8, i.e. (10 −2 = 8, 11 −3 = 8, 9 −1 = 8, 12 −4 = 8). THE ACTUAL ADDRESS ASSIGNMENTS ARE ARBITRARY. NOTE THAT MORE THAN ONE P. ROM WORD CAN BE USED FOR A GIVEN STATE ASSIGNMENT TO IMPLEMENT A FLOWCHART.



2-4/10M/N

ROM IN SEQUENTIAL & COMBINATORIAL LOGIC

APPLICATION NOTE 102

Monolithic Memories INCORPORATED

INTRODUCTION

Since the first semiconductor ROM was made available some three years ago, there has been some apprehension on the part of many potential users as to the feasibility of using ROM's. These apprehensions were aroused because of ROMs being considered custom LSI chips and only economical in large quantities. There also existed the fear of mask charges and turn around time. The need for prototyping was obvious, and with the introduction of the programmable Read Only Memory, a prototyping tool became available.

Monolithic Memories pioneered the pin and performance compatibility between ROM and programmable read only memory (PROM). The PROM was considered by most of the industry to be a twin prototype to a mask ROM. There are many other effective uses of inter-mixing mask ROM's with programmable ROM's, for instance, in applications that require periodic changes. Many designers have long recognized the powerful logic replacement that ROM' s could perform but have stayed away from the concept because of low quantity, one of a kind applications. However, the availability of programmable ROM's in low quantities has made other PROM type applications feasible.

It is the intention of this application note to show other non-CPU or non-microprogramming uses of PROM's/ ROM's. The use of PROM's in each concept can be substituted with ROM's. The feasibility of the substitution is based on the ultimate quantity of the application of each one of the concepts.

COMBINATORIAL LOGIC FUNCTION

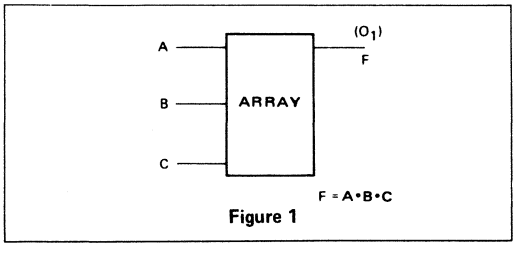


Figure 1

COMBINATORIAL LOGIC FUNCTION (See Fig. 1)

Booleon functions such as "AND", "OR", "NAND", "NOR" can be programmed with ROMs or PROMs. The expression should first be simplified to aid in transposing the terms into ROM address. "AND" terms are simple gating functions and are implemented simply by transposing the number of "AND" terms into ROM addresses. For example, A•B•C equal address seven of a ROM or binary 111.

SEQUENTIAL LOGIC FUNCTION

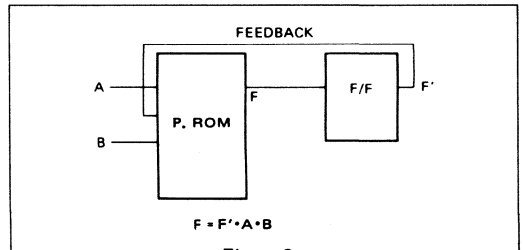


Figure 2

SEQUENTIAL LOGIC FUNCTIONS (See Fig.2)

Basically, sequential logic functions require some steady state constant as a basis to include another variable function, whose derivative or output function is still a second function which is then reapplied to the device as the next basic constant. For instance, refer to Figure 2, more satisfactorily called a Feed Back Function. A very common example of sequential logic is a synchronous counter.

Monolithic Memories INCORPORATED

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TWX 910–339-9229

DECEMBER 1971

COMBINATORIAL LOGIC FUNCTION

$A \oplus B \quad C \oplus D = F_4$
$A + B + C + D = F_3$
$A \cdot B \cdot C \cdot D = F_2$
$A \cdot B + C \cdot D = F_1$

FUNCTION						F_1	F_2	F_3	F_4
ADDRESS	A_0	A_1	A_2	A_3	OUTPUT	O_1	O_2	O_3	O_4
0	0	0	0	0		1		1	
1	1	0	0	0		1		1	
2	0	1	0	0		1		1	
3	1	1	0	0		1		1	
4	0	0	1	0				1	
5	1	0	1	0				1	1
6	0	1	1	0				1	1
7	1	1	1	0		1		1	
8	0	0	0	1				1	
9	1	0	0	1				1	1
10	0	1	0	1				1	1
11	1	1	0	1		1		1	
12	0	0	1	1				1	
13	1	0	1	1				1	
14	0	1	1	1				1	
15	1	1	1	1			1	1	

SYNCHRONOUS COUNTER

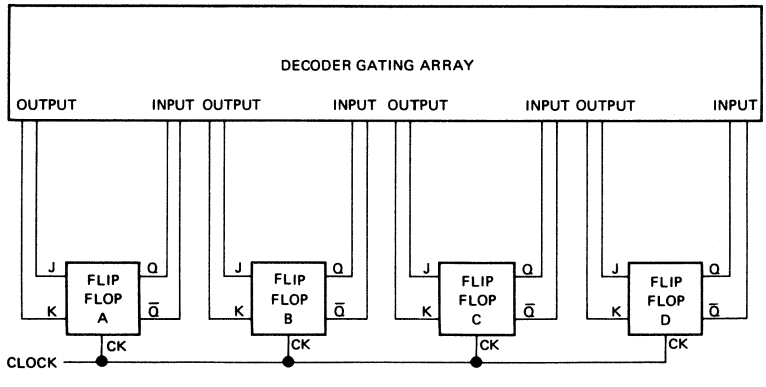


Figure 3

SYNCHRONOUS COUNTER (See Fig. 3)

Let's look at a synchronous counter and make some evaluations (see diagram). In the synchronous counter all flip-flops change state simultaneously with the application of a clock. The storage state of the flip-flops is sensed through a gating array and decoded into the next count. This count is at the JK input of the flip-flop waiting to change the state of the flip-flop when the next clock pulse is applied. Replacing the normal gating array with a ROM we can decode the state of the flip-flop, enabling the JK inputs with the next count. The count is transferred to the flip-flop with the application of clock.

PROMS AS SYNCHRONOUS COUNTERS

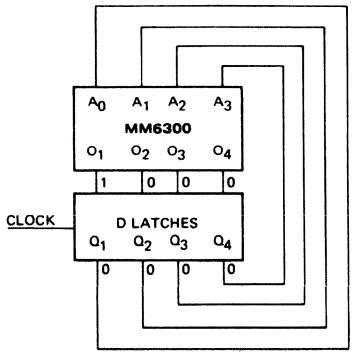


Figure 4

PROMS AS SYNCHRONOUS COUNTERS (See Fig. 4)

Now that we see the operation of a synchronous counter, we can make some substitution. Instead of a decoder we substitute a PROM such as the MM6300. In place of JK flip-flops we use "D" latches and by programming a PROM with the proper up count code starting with address zero as count one. Initially the "D" latch outputs are low, addressing the ROM as address zero. Address Zero propagates through the PROM to access the programmed information (which for the sake of this discussion is 1000). This data is waiting to be applied to the "D" latches with the application of clock. When clock is applied to the "D" latch the latches store 1000 and also apply this data to the address of the PROM or ROM as a new address to access a new program data word. This procedure is repeated again for the next count.

The following application of PROMs includes an example Truth Table. The entire Truth Table was not included in each case. The purpose of the Truth Table is to show the feasibility of the application.

COUNT SEQ SELECT	A_4	A_5	A_6	COUNT FUNCTION
1	0	0	0	BINARY UP
2	1	0	0	BINARY DN
3	0	1	0	BCD UP
4	1	1	0	BCD DN
5	0	0	1	GRAY CODE
6	1	0	1	ETC
7	0	1	1	ETC
8	1	1	1	ETC

Figure 5

SYNCHRONOUS COUNTER (Cont'd)

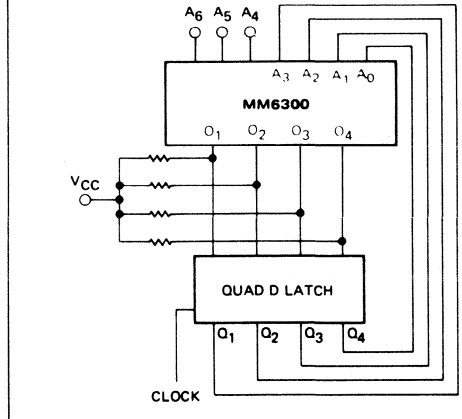


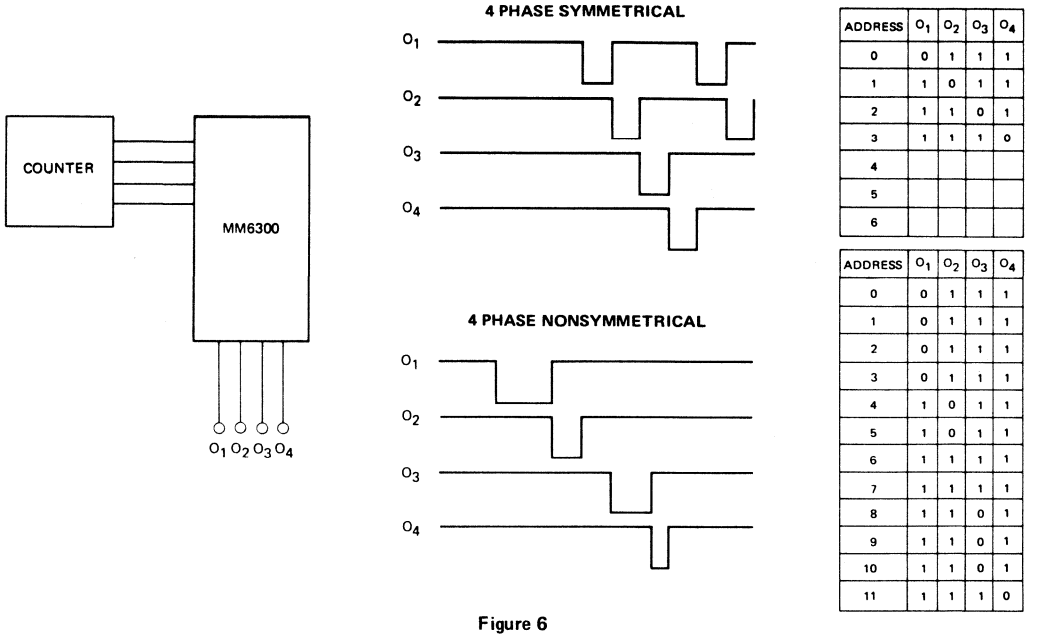
Figure 5 (Cont'd)

SYNCHRONOUS COUNTER (See Fig. 5)

The application of a 6300 PROM being utilized to make a binary up, binary down, BCD up, BCD down and a gray code counter. The 6300 PROM is programmed in a count sequence that addresses A0 through A3, with A4, A5 and A6 held at 0 as a straight binary up count, if address A1 is high. The PROM is now placed in a new quadrant and the new information is now programmed to be a binary down count. As can be seen with A4 through A6 utilized, the field of eight (8) different count sequences can be established with given sequence information of up to a 16 bit count. Any particular sequences can be utilized with 6330 and other PROM devices to form complete synchronous counter of up to eight (8) bits. The device has the unique capability of being expandable in bit length, with a complete synchronous count up to the capacity of the amount of bits of the PROM.

The following application functions can be programmed easily for breadboard prototypes with PROMs. They may be simple one-of-a-kind uses. The purpose of this application is to show that PROMs have other uses that fulfill one-of-a-kind functions. ROM can be substituted wherever quantity or uniqueness of application details their use, such as, (1) low package count; (2) quick change over; and (3) a powerful in-house logic tool for reduced inventory of unique MSI functions.

MULTIPHASE CLOCK GENERATION



ADDRESS	O_1	O_2	O_3	O_4
0	0	1	1	1
1	1	0	1	1
2	1	1	0	1
3	1	1	1	0
4				
5				
6				

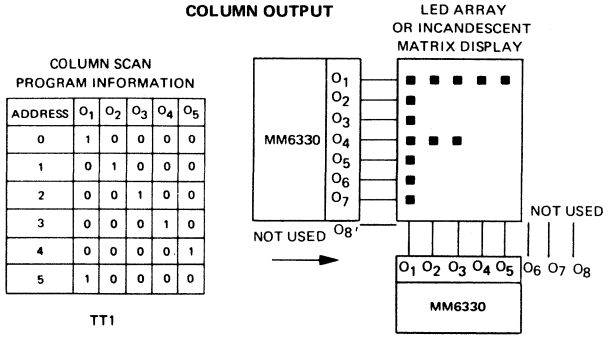
ADDRESS	O_1	O_2	O_3	O_4
0	0	1	1	1
1	0	1	1	1
2	0	1	1	1
3	0	1	1	1
4	1	0	1	1
5	1	0	1	1
6	1	1	1	1
7	1	1	1	1
8	1	1	0	1
9	1	1	0	1
10	1	1	0	1
11	1	1	1	0

Figure 6

MULTIPHASE CLOCK GENERATION (See Fig. 6)

Multi Phase Clock Generation can be accomplished with the 6300. It can be programmed to supply complex 4 phase clock functions or to other MOS RAM devices that require multiple phases. The simplest way to accomplish multiple phase decodes of different time durations to satisfy complex wave forms is to program the PROM as shown in Figure 6. The pulse width for a 1 bit programmed into the PROM is established by the clock rate of the counter cycling the 6300. The rep rate of that pulse is the amount of bits utilized in a full scan.

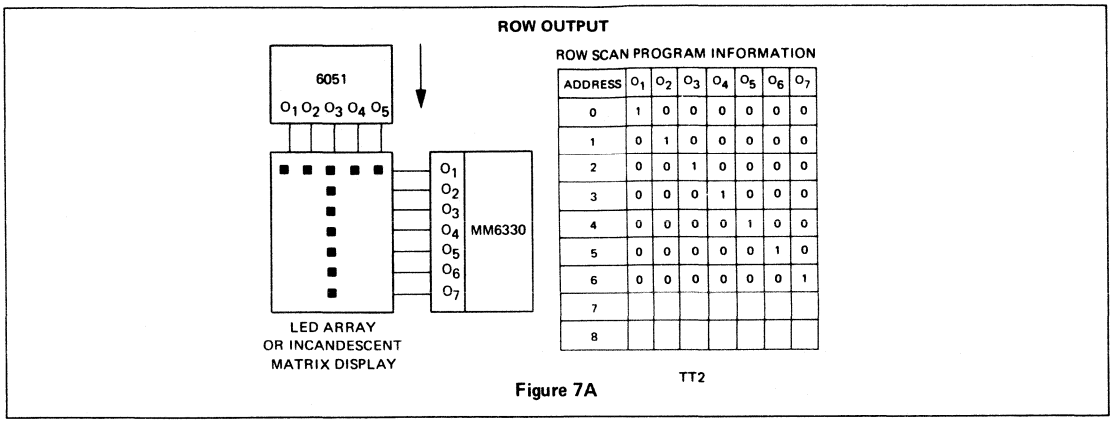
5 X 7 FIXED FONT LED OR INCANDESCENT ARRAY



ADDRESS	O_1	O_2	O_3	O_4	O_5
0	1	0	0	0	0
1	0	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	0	0	0	0	1
5	1	0	0	0	0

Figure 7

5 X 7 FIXED FONT LED OR INCANDESCENT ARRAY



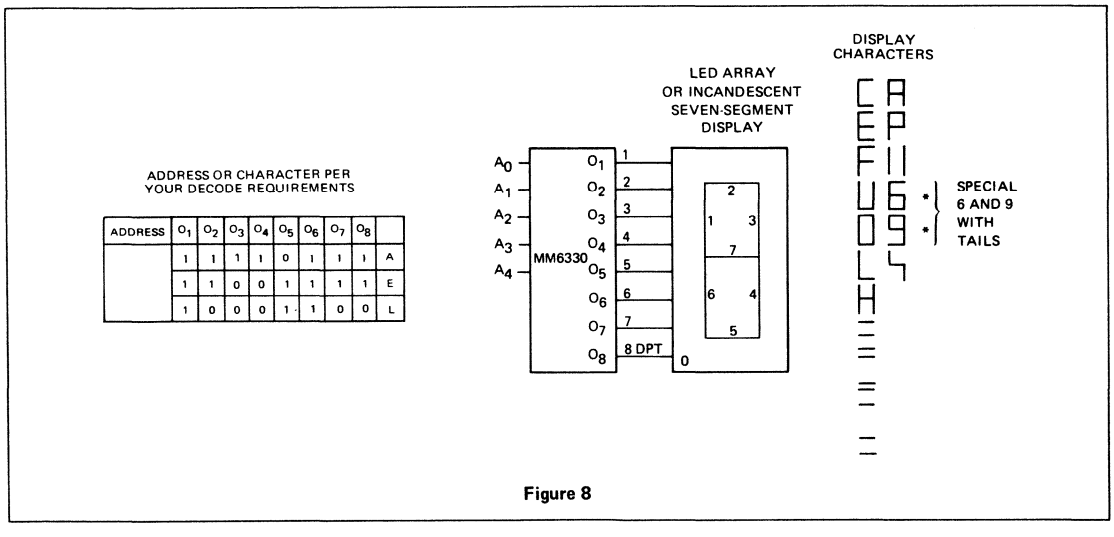
ADDRESS	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0
2	0	0	1	0	0	0	0
3	0	0	0	1	0	0	0
4	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0
6	0	0	0	0	0	0	1
7							
8							

Figure 7A

5 X 7 FIXED FONT LED OR INCANDESCENT ARRAY (See Fig. 7 & 7A)

Shows the utilization of a 5 x 7 character generator such as the 6051 (Fig. 7A). The 6051 supplies the row output information to the LED or incandescent array, and by programming a 6330 PROM to Truth Table 2 an enabling scan can be generated to produce the 5 x 7 row output character display. Likewise, utilizing a column scan device (Figure 7), the 6330 can be programmed now to accomplish the field scan in the opposite direction, as per Truth Table 1. Secondary considerations in utilization of open collector ROM is the higher voltages that can be used to interface with a wide variety of displays. LED and incandescent display up to 12 VDC.

7 SEGMENT LED ARRAY or INCANDESCENT



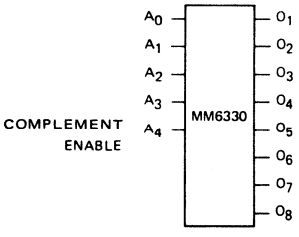
ADDRESS	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	
	1	1	1	1	0	1	1	1	A
	1	1	0	0	1	1	1	1	E
	1	0	0	0	1	1	0	0	L

Figure 8

7 SEGMENT LED ARRAY or INCANDESCENT (See Fig. 8)

The MM6330 can be programmed as a seven segment decoder driver, with some extra advantages not available in MSI units. Since the MM6330 has a capacity of 32 words some special symbols can be displayed such as the ones listed above. In addition, 6's and 9's can be programmed with tails, which are not available from many MSI decoder manufacturers. Six's and nine's with tails are aesthetically more pleasing in a display.

OCTAL DECODER



COMPLEMENT ENABLE — OCTAL INPUT — OCTAL DECODE

A_4	A_3	A_0	A_1	A_2	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
0	0	0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	0	0	1	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0	0	0	0	1	0
0	0	1	1	1	0	0	0	0	0	0	0	1
0	1	0	0	0	0	1	1	1	1	1	1	1
0	1	1	0	0	1	0	1	1	1	1	1	1
1	X	X	X	X	1	1	1	1	1	1	1	1

Figure 9

OCTAL DECODER (See Fig. 9)

A simple octal decoder can be made with a PROM, with the expanded ability to complement the output function.

PARITY GENERATOR, PARITY CHECKER

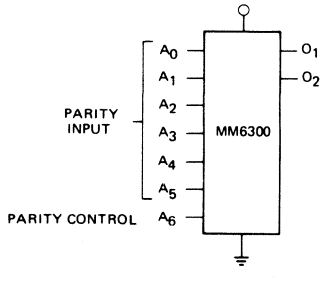
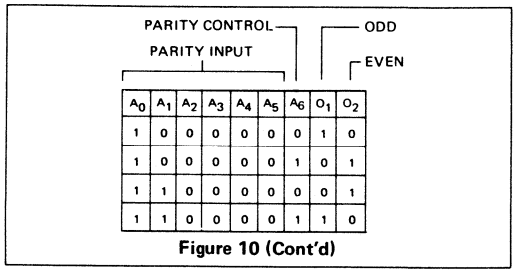


Figure 10

PARITY GENERATOR, PARITY CHECKER (Cont'd)



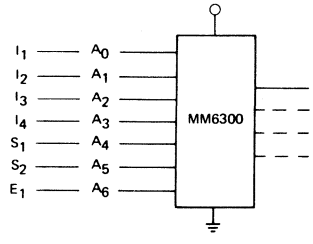
A_0	A_1	A_2	A_3	A_4	A_5	A_6	O_1	O_2
1	0	0	0	0	0	0	1	0
1	0	0	0	0	0	1	0	1
1	1	0	0	0	0	0	0	1
1	1	0	0	0	0	1	1	0

Figure 10 (Cont'd)

PARITY GENERATOR, PARITY CHECKER (See Fig. 10)

The 6300 can again be programmed to utilize it for parity checking and parity generation. The A6 control line (A6 address line) is used as a parity control line to set whether odd or even parity will be checked. The O1 or O2 outputs are complemented functions of each other. One is used for odd parity, the other one is used for even.

MULTIPLEXER



I_1 I_2 I_3 I_4 S_1 S_2 ENABLE

A_0	A_1	A_2	A_3	A_4	A_5	A_6
0	0	0	0			
1	0	0	0			
0	1	0	0			
1	1	0	0			
0	0	1	0			
1	0	1	0			
0	1	1	0			
1	1	1	0			
0	0	0	1			
1	0	0	1			
0	1	0	1			
1	1	0	1			
0	0	1	1			
1	0	1	1			
0	1	1	1			
1	1	1	1			

Figure 11

MULTIPLEXER (See Fig. 11)

The 6300 can also be utilized as a 4 input multiplexer. Given the information of the control states of A0 through A3, utilized as inputs and A4 and A5 utilized as select controls, A6 as an enable. Another scheme can be compiled by the user and programmed into the PROM to establish other multiplexer schemes. All given states have four inputs, which will be reflected to the outputs by a scan condition of A4 and A5. A6 can be utilized to put the PROM in the last field or as an enable function to turn the device on or off.

SIMPLE D/A CONVERTER, DIGITAL TO ANALOG

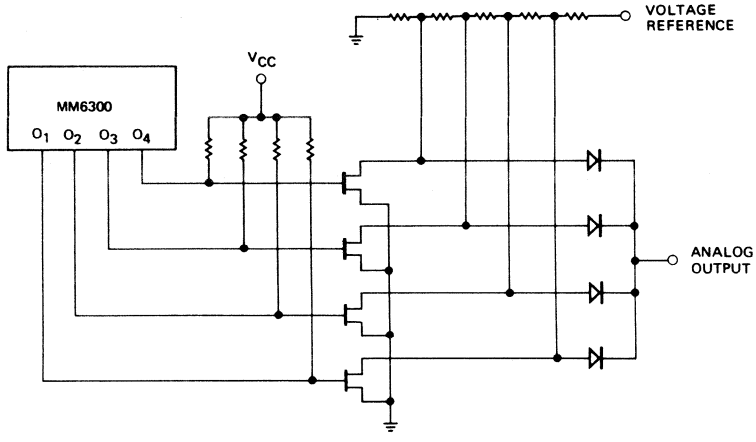


Figure 12

SIMPLE DIGITAL TO ANALOG CONVERTER

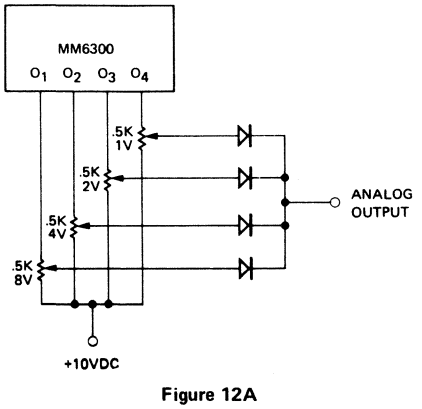
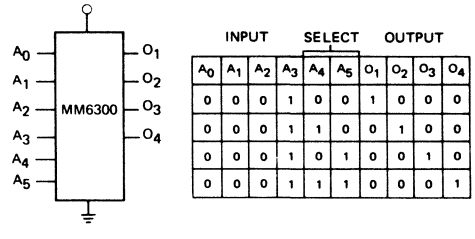


Figure 12A

SCALER



INPUT				SELECT		OUTPUT			
A_0	A_1	A_2	A_3	A_4	A_5	O_1	O_2	O_3	O_4
0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	0	0
0	0	0	1	0	1	0	0	1	0
0	0	0	1	1	1	0	0	0	1

Figure 13

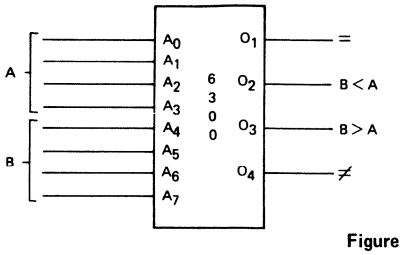
SIMPLE DIGITAL TO ANALOG CONVERTER (See Fig. 12 & 12A)

A 6300 or 6330 can be utilized with V_{CC}'s on the output of up to 12 volts. Since it truly is a decoder, the selection of the bit program is strictly up to the user. Schemes of simple D to A can be performed by the 6300 or the 6330.

SCALER (See Fig. 13)

The 6300 can also be utilized as a 4 bit scaler or a shift register function. For information placed on its input can be shifted any direction and positioned 1 to 4 different bit positions. Again, A4 and A5 are used as selector bits to establish the select command for moving the bits from left to right.

4 BIT COMPARATOR



A IN				B IN				B ≠	>A	<A	=
A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	O_4	O_3	O_2	O_1
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	0	0	1	1	0	0
1	0	0	0	1	0	0	0	0	0	0	1
1	1	0	0	1	1	0	0	0	0	0	1
1	1	1	0	1	1	1	0	0	0	0	1
LSB A				LSB B				COMPARATOR OUTPUT			

Figure 14

4 BIT COMPARATOR (See Fig. 14)

Address input A_0 – A_3 are used as A input. Address A_4 – A_7 are used as B inputs. Outputs O_1 is the B equal to A output. Output O_2 is the B less than A output. Output O_3 is the B greater than A output. Output O_4 is the B unequal to A output.

CRT CLOCK DISPLAY

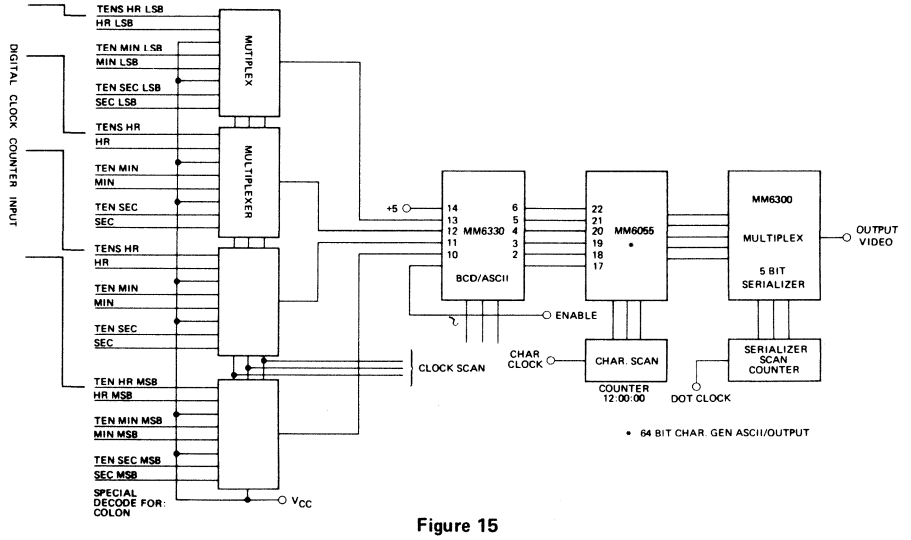


Figure 15

CRT CLOCK DISPLAY (See Fig. 15)

A scheme for utilizing the 6330 with the 6055 with a Digital Clock Display to display the real-time clock information on a CRT display. The 6330 accomplishes the decoding job of selecting the right numeric functions for the 6055 to generate this clock function. A special high logic functions, into the multiplexers, is utilized to generate a colon as separators between the digits of the clock.

Monolithic Memories
INCORPORATED

article reprint

Shift registers can be designed using RAMs and counter chips

Here are techniques for building large, high-speed, variable-length shift registers with economical RAM and counter components.

David C. Wyland, Monolithic Memories, Inc.

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Shift registers are widely used in electronic systems and as a result, designers are always looking for novel and improved ways of implementing them. This is particularly true when the shift-register application calls for large size, high speed or programmable length. One way of implementing the shift-register function to provide these desired characteristics is to use random-access memories (RAMs) in conjunction with counters.

Fig. 1 shows the operation of a 4-bit shift register. The contents of the last shift-register bit, bit 3, are available at the output, and the first bit, bit 0, is prepared to receive the next data bit. Application of a clock pulse causes the input data to be loaded into bit 0, bit 0 to be loaded into bit 1, bit 1 into bit 2, and bit 2 into bit 3. The previous contents of bit 3 are lost. If the output of bit 3 is tied to the input of bit 0, bit 0 will be loaded with the contents of bit 3, and no data will be changed or lost. This is called a recirculating shift register. The output of a 4-bit recirculating shift register will be a sequence of bit 3, 2, 1, 0, 3, etc., repeating every four clock pulses.

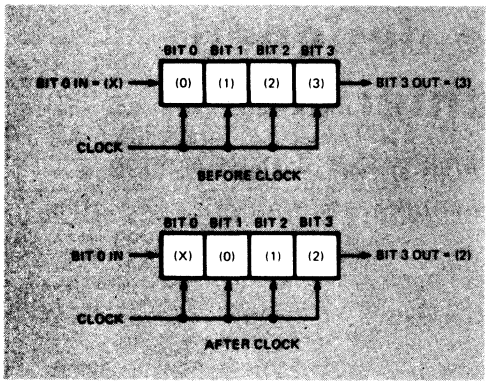

Fig. 1—Four-bit shift register moves data sequentially from bit position 0 to 1 to 2, etc.

A RAM and counter does it too

A combination of a 4-word, 1-bit RAM and a 2-bit counter can be made to give the same output as a 4-bit recirculating shift register. If a 2-bit, decrementing counter is used to address a 4-bit RAM and the counter is stepped by each clock pulse, the RAM output will be the contents of location 3, 2, 1, 0, 3, etc., in the same manner as a 4-bit recirculating shift register. If an incrementing counter is used, the outputs will appear in reverse order; i.e., 3, 0, 1, 2, 3, 0, etc. If a bidirectional counter is used, a bidirectional recirculating shift register is formed, with "right shift" corresponding to counter decrement and "left shift" corresponding to counter increment. A diagram of such a RAM and counter and its operation is shown in **Fig. 2.**

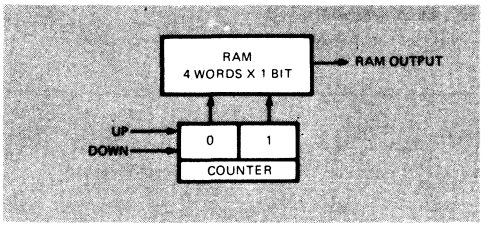

Fig. 2—A 4-bit, recirculating shift register can be made from a 4-word by 1-bit RAM and a 2-bit counter.

To load one bit of a 4-bit recirculating shift register, the bit-0 input is switched from the bit-3 output to the data input for one clock period. The new data is loaded into bit-0 and the old, bit-3 data is lost. This is shown in **Fig. 3.** After three more clock pulses, the shift register will have returned to the original state which existed immediately previous to loading of the new data bit. The old bit-3 information has been replaced by the new data bit and the other bits remain unchanged.

To load our recirculating RAM-counter shift register, the old output bit is overlaid with the new data. This is done by enabling the write gate of the memory with the clock pulse, as shown in **Fig. 4.** A latch is added to the RAM output to prevent the shift register output from changing during the clock pulse. Selection of load or recirculate is performed by enabling or disabling the RAM write pulse.

If a programmable counter is used with a RAM, a variable-length shift register results. This is shown in **Fig. 5.** A pair of 74163 synchronous reset counters are used to drive a 256-word, 1-bit RAM and a decoder. When the desired last count value is reached, the decoder activates the 74163 synchronous reset inputs and the counter is reset to 0 by the next clock pulse. Thus, a sequence of 0, 1, 2, . . . 137 138, 0, etc., may be implemented.

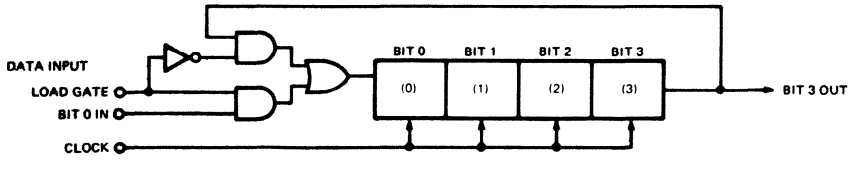

Fig. 3—A new bit is loaded into a 4-bit recirculating shift register by disconnecting the bit-0 input from the bit-3 output and connecting it for one clock period to the data input.

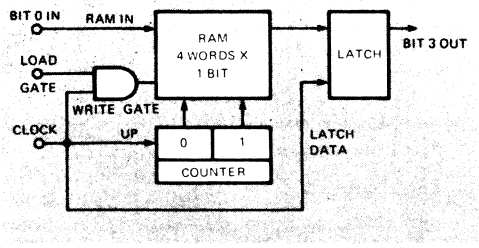

Fig. 4—Enabling or disabling of the WRITE gate determines whether data will be loaded into the RAM-counter shift register or whether the output bit will be recirculated.

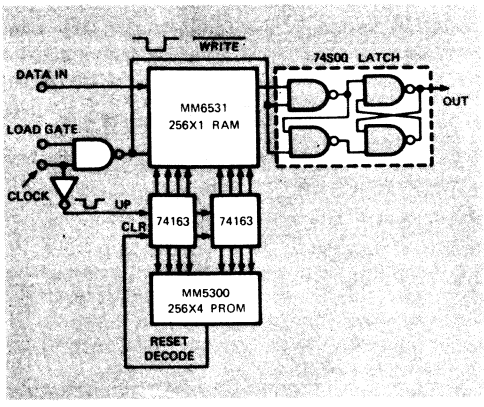

Fig. 5—A variable-length shift register results when a programmable counter is used with the RAM. One such method uses synchronous reset counters in conjunction with a programmable ROM.

This is equivalent to a nonbinary length shift register with the length determined by the decoder. By using a programmable ROM for the decoder, the register length can be easily changed. If comparator chips, such as 7485's are used in place of the decoder, the shift-register length can be varied during use and controlled by other logic, as shown in **Fig. 6.**

Performance of the RAM-counter shift register is shown in **Fig. 7.** Minimum clock-pulse spacing for the shift register in the recirculate mode is the sum of the settling time of the counter, the address access time of the RAM, and the set-up time of the latch. The minimum clock spacing in the load mode adds the minimum RAM write-pulse width to the clock-pulse time for the recirculate mode (**Table 1**).

Large RAM-counter systems which use several RAM chips require decoding of the higher order bits of the counter for enable selection of the RAM chip currently active. An enable decoder will increase the effective access time of the RAM if the decoder propagation delay exceeds the difference between the RAM address access time and enable access time. To avoid this degradation in performance, buffer registers such as the

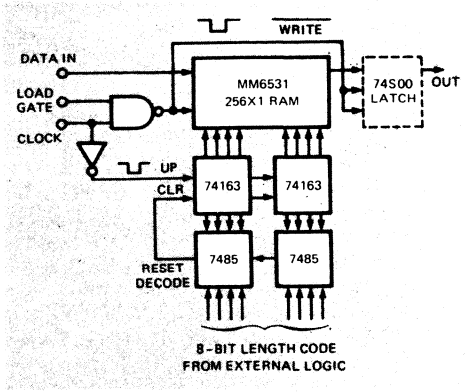

Fig. 6—Comparator chips controlled by external logic can also be used to provide programmable operation of the shift register.

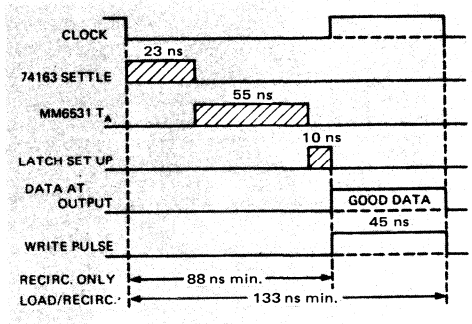

Fig. 7—Timing diagram for RAM-counter shift register shows clock pulse relationship between recirculation and load modes.

TABLE I

MINIMUM CLOCK SPACING FOR RAM–COUNTER SHIFT REGISTER

	COMMERCIAL		MILITARY	
DELAY ELEMENT	LOAD	RECIRC.	LOAD	RECIRC.
74163 SETTLE	23	23	23	23
RAM ACCESS	55	55	70	70
LATCH SET UP	10	10	10	10
RAM WRITE	45	—	55	—
	133 ns	88 ns	158 ns	103 ns

74S175 may be inserted between the counter and enable decoder and the RAMs. A 4096-bit RAM-counter system with counter buffering is shown in **Fig. 8.** The timing of such a system for both buffered and unbuffered operation is shown in **Table 2.**

Multiplexing increases speed

The speed of the RAM-counter shift register can be increased by multiplexing. This consists of using two slow shift registers in an alternate fashion to simulate a single shift register of twice the speed capability of the slower ones. The only limitation is that the simulated shift register must be an even number of bits in length.

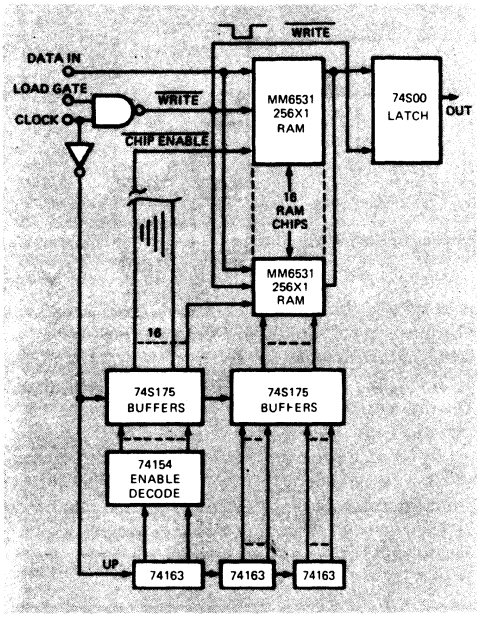

Fig. 8—The use of buffer registers improves the effective access time in systems that require several RAM chips.

TABLE 2

MINIMUM CLOCK SPACING: BUFFERED VS. UNBUFFERED		
DELAY ELEMENT	UNBUFFERED	BUFFERED
74163 SETTLE	23	–
74S175 SETTLE	–	11
74154 NET DELAY	16	–
6531 RAM ACCESS	55	55
74S00 LATCH	10	10
6531 RAM WRITE	45	45
	149 ns	131 ns

TABLE 3

MINIMUM CLOCK SPACING FOR 8192-BIT MULTIPLEXED UNIT	
DELAY ELEMENT	UNBUFFERED DELAY
74163 SETTLE	23
74154 NET DELAY	16
6531 RAM ACCESS	55
74S00 LATCH	10
6531 WRITE	45
	149
DIVIDE BY 2 FOR MULTIPLEXING	2
	75 ns

Fig. 9 shows an 8192-bit, 75-nsec multiplexed shift register formed from two 4096-bit, 149-nsec RAM-counter shift registers. The timing analysis for the shift register of **Fig. 9** is shown in **Table 3**.

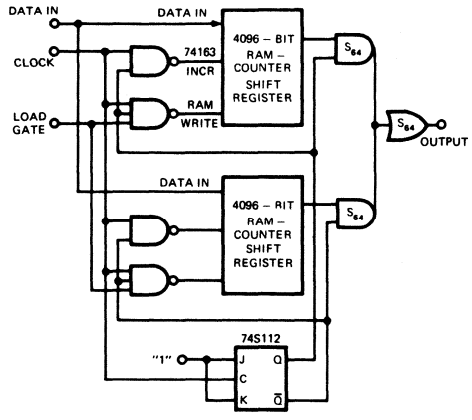

Fig. 9—An 8192-bit RAM-counter shift register can be formed by multiplexing two 4096-bit shift registers. The multiplexing operation is controlled by the 74S112 flip-flop.

The multiplexed shift register of **Fig. 9** is programmable in length in the same fashion as earlier described. Programmed length is accomplished by programming the length of the individual RAM-counter shift registers. Both RAM-counter shift registers must be programmed to the same value, which is exactly half the desired length of the multiplexed system.

In the multiplexed design of **Fig. 9**, one of the two component shift registers is accessing data while the other is reading out previously accessed data. The 74S112 flip-flop selects which shift register will be read out from and written into, and which shift register will be settling to its new address from the previous clock pulse. The timing of the individual shift registers remains unchanged except that they are clocked every other cycle. Data is available at the output for at least one clock width (less the delay of the 74S64) in the minimum clock spacing case. The timing of the 74S112 does not enter into the calculations since it merely gates the clock signal. The only timing requirements are those of minimum clock spacing and minimum clock-pulse width equal to the minimum RAM write pulse. □

Author's biography

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Memory Systems Terminology

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Memory systems

terminology

by Joseph J. McDowell, Monolithic Memories, Inc.

Do you understand the meaning of the terms read cycle, write cycle, fetch cycle, access time, store cycle nondestructive readout, interleaving?

SEMICONDUCTOR COMPONENT manufacturers specify access and recovery times for their memory products. Core memory system buyers, on the other hand, talk in terms of fetch and store cycles and find it hard to understand how a semiconductor memory can have an access time of 200 nsec and a read cycle of 100 nsec. In core memories, this situation could usually result only from interleaving. As a result, the component or system customer often places unwarranteed emphasis on access/cycle specifications and does not use the full performance capabilities of a semiconductor memory. We will show the relationship between component specifications and system timing diagrams, suggest definitions for commonly used performance specifications of a semiconductor memory, and indicate which specifications are important for a particular application.

Component specifications

Figure 1 shows a typical specification for a memory component used as a high-speed buffer, local store, or scratchpad. Address and enable access times, write pulse width, and recoveries are specified. Let us discuss each of the specified terms and see how they relate to read and write cycles and performance in a large memory system.

Access time

Access time is defined as the time delay at specified thresholds, from the presentation of an enable or address input pulse until the arrival of the memory data output. The memory should be cycled at a read cycle, to be defined later, which is substantially slower than the specified minimum read cycle to avoid read cycle/access time interactions.

Enable-to-output access time (which assumes the address is stable) rather than the address-to-output access time (which assumes the memory is enabled all the time) is the important parameter in random access memories (RAM's) used in large memory systems. Pulse skews, race conditions, and cabling delays in large systems do not, in general, permit keeping the memory enabled all the time. This condition occurs because of false writes into the addresses at the beginning and end of memory cycles, as shown in Fig. 2. In read only memories (ROM's), however, stored data cannot be changed under any combination of skew or race conditions, so we can be legitimately concerned about address-to-output access time. When ROM's are wire-OR'ed together to form longer word length, enable access time is important since it may be used to decode the desired address.

Often, typical access times or maximum access times are specified at nominal voltage and 25°C. These figures are useless since a system can only be designed on the basis of maximum access time at worst-case voltage and temperature. Access variations may vary between products that are "spec-for-spec, pin-for-pin compatible."

How large a variation in access time exists in a typical bipolar product today? Monolithic Memories has found that the variation typically will be ⅓ or ½ the specified maximum access time at nominal voltage and temperature, and that voltage and temperature variations will add 10% to 20% to the maximum nominal access time.

GUARANTEED LIMITS @ (T_A = 25°C, V_{CC} = +5.0v, Std. Load)			MM5500/6500			MM5501/6501			
Test	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Units
Address Access Time	t_{AA}	WE = "1" Logic "1" Stored		45	60		40	50	nsec
Enable Access Time	t_{EA}	WE = "1" Logic "1" Stored		45	60		40	50	nsec
Address and Enable Recovery Time	t_{AR} and t_{ER}	WE = "1" Logic "1" Stored		25	40		25	40	nsec
Write Pulse Width	t_{WP}	Address Fixed	25	15		25	15		nsec
Write Recovery Time	t_{WR}	E = "0"		−20	0		−20	0	nsec
Output Write Recovery Time	t_{OWR}	Address Fixed D_X = "0" or "1"		45	60		40	50	nsec

Fig. 1. Switching characteristics of a typical semiconductor memory component — a 64-bit RAM (MM5500/5501).

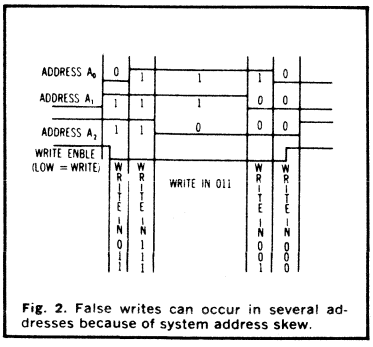


Fig. 2. False writes can occur in several addresses because of system address skew.

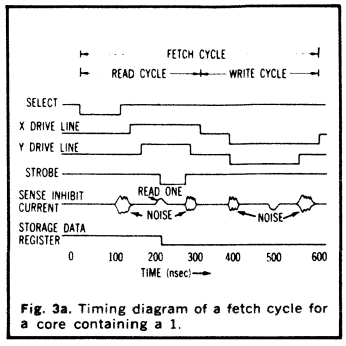


Fig. 3a. Timing diagram of a fetch cycle for a core containing a 1.

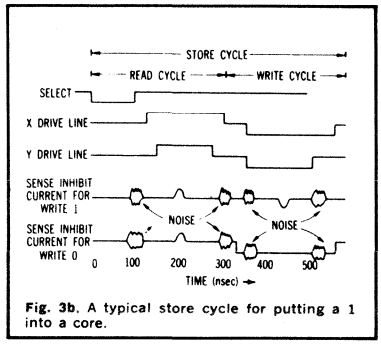


Fig. 3b. A typical store cycle for putting a 1 into a core.

Storage cycle time

Most of the problems involved with understanding storage cycle time arise from previous associations with core memories, or in assuming that cycle time and access time are synonomous. In a core memory, fetch cycle is destructive and it is necessary to write (regenerate) the information back into the core after a readout. Every core fetch cycle is a read cycle plus a write cycle. Similarly, the core store cycle is a read cycle to clear the core to ZERO, followed by a write-only in cores to be set to the ONE state.

Fetch cycle

Figure 3a shows a fetch cycle for a core containing a 1. Our objective is to sense a 1 and set the storage data register to a 1. During the write half of the cycle, the core is selected by the X and Y lines, as in the read half of the cycle, but the write current changes the core from 0 to 1.

During the first half of the fetch cycle (the read half) we destructively read a 1, and during the second half of the fetch cycle (the write half), the 1 is restored to the core.

Store cycle

Figure 3b shows a store cycle for putting a 1 into core. During the read half of the cycle, the core is cleared by the destructive readout. Whether a 1 or 0 is stored is irrelevant; there is no strobe to allow entry into the storage data register.

A 1 on the data-in line during the write half of the cycle will write a 1 into the location selected by the X and Y lines. Note that the inhibit-driver current polarity determines whether a 1 or 0 is written into the core.

Interleaving

In order to decrease the storage cycle time in memory systems, we divide the memory into two independent even and odd sections and wire-OR the outputs together by routing the select signal to the odd or even memory section, depending on the state of the least significant address digit. This method enables us to start an even cycle, for example, before the previous odd cycle is complete. This even and odd memory subdivision technique is called interleaving.

When a memory with a 750 nsec storage cycle is interleaved, a second storage cycle can be started 375 nsec after the first cycle. This sequence is shown in Fig. 4. For the case where an even cycle is followed by an even cycle or an odd cycle is followed by an odd cycle, we must wait the full 750 nsec. Since the program counter in the central processing unit (CPU) loads the memory sequentially (even, odd, even, odd, etc.), the odds are that we will see something close to 375 nsec vs the typical storage cycle time.

For the case with multiple CPU's, the odds of a 375 nsec cycle are improved. For example, if CPU 1 starts an even cycle at time ZERO and executes another even cycle, a 750 nsec cycle results, since an even cycle is followed by an even cycle. CPU 2 or CPU 3, etc. (if it has an odd cycle), can be started at 375 nsec, increasing system thruput.

Access time of the memory is not improved by interleaving, since access time is the delay through the even or odd memory, shown as 400 nsec in Fig. 4. Access time is far more important than cycle time when comparing memory systems, because interleaving can always be used to decrease cycle time.

Nondestructive readout

When a memory can be read without destroying the stored information, it is said to possess nondestructive readout. Most solid-state memories have nondestructive readout (NDRO) since

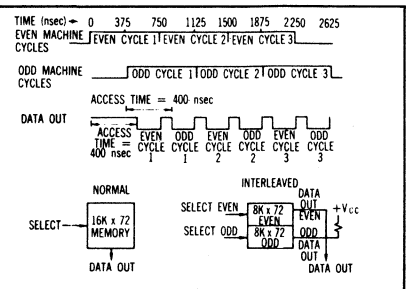


Fig. 4. An interleaved memory has 2 independent even and odd sections wire-OR'd together.

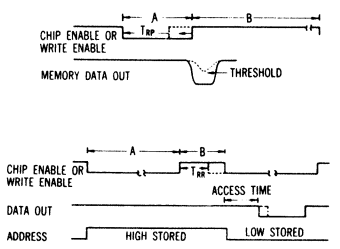


Fig. 5. Step 1 in getting a minimum read cycle is determining T_{RP} at B = 10A. Step 2 is to determine T_{RR} at A = 10B.

cross-coupled transistor flip-flops are employed for storage. These units are designed so that the state of the flip-flop can be determined without changing its state. Cycle times (both read and write) can be independent of access time in a semiconductor memory when it is operated slower than the minimum specified cycle time.

In core memories, the delay in getting the data out of the core (access time) is an integral part of the fetch cycle since the data has to be restored in the last half of the cycle, thus complicating interface timing.

Minimum read cycle

The minimum time interval between successive addresses when the write-enable (instruction) line is in the read state is defined as the minimum read cycle. The minimum read cycle must be determined in two steps, as shown in Fig. 5 and explained below, to isolate the pulse width required when the memory is active from recovery limitations. The 64-bit RAM shown in Fig. 1 is used as an example.

1. Narrow the chip enable, or write enable pulse width A, until the data output does not reach threshold with B set at 10 times A. It is obvious that the memory cannot be operated with a pulse width narrower than this because of internal skews due to capacitive loading and band width limitations. This parameter is called minimum read pulse width — T_{RP}. The 64-bit RAM of Fig. 1 has a T_{RP} of 20 nsec.

2. Make A 10 times B and load the memory so that a 1 will be read out of address M and a 0 will be read out of address N. Decrease the pulse width B until the access time of address N just starts to increase, in order to study at what point recovery from the previous cycle starts to affect access time. Repeat the process with the memory loaded so that a 0 will be read from address M and a 1 will be read from address N. Decrease the pulse width of B until a glitch appears in normal high readout of address N which is below the next stage's threshold (1.5 v for TTL). The maximum of the 2 minimum values of B is called read recovery — T_{RR}. The memory was loaded with opposite data in addresses M and N to offset the on-chip sense amplifier so that the recovery would be maximum. The 64-bit RAM gives a T_{RR} of 30 nsec. Minimum read cycle is the sum of T_{RP} and T_{RR}, or 20 + 30 = 50 nsec.

Minimum write cycle

The minimum time interval between successive address presented to the memory when the write-enable (instruction) line is in the write state is defined as the minimum write cycle. Minimum write cycle is determined in two steps in order to isolate the controlling parameters.

1. Load address M with a 1. With the address and chip-enable d-c selected and the data in the proper state for a 0 readout, widen the write-enable pulse from zero nsec until the memory readout gives a 0. Repeat the process with address M having a 0 stored initially, and change the stored information to a 1. The maximum of the 2 write pulse widths is T_{WP} and is 25 nsec on Fig. 1's data sheet.

2. Widen the write-enable ON time to 10 times T_{WP} or 250 nsec, and determine the OFF-time by measuring output recovery time from system noise. We must wait for this recovery in the case of a write cycle followed by a read cycle, since the access time of the read cycle assumes write recovery is complete. This parameter is called T_{OWR} and is specified at 50 nsec in Fig. 1.

3. Minimum write cycle is T_{WP} + T_{OWR} or 25 + 50 = 75 nsec. Write cycle is not as important as read cycle in memory systems; about 70% of machine cycles are read cycles. — *J/L*

HOW TO DESIGN YOUR OWN MICROCOMPUTER

By: *DAVE WYLAND*
June 26, 1974

A computer is a memory controller. Its function is to move and combine data in the memory unit it controls. A computer can be used as a universal digital interface if the equipment being interfaced is made to look like computer memory. In the current controversies over computers, minicomputers, and microcomputers, these simple definitions tend to be overlooked.

All computers are basicly alike. The only difference among them is the size and speed of the memory controlled, the efficiency with which the data can be moved or combined relative to a given application, and peculiar restrictions on interfacing I/O devices. Even today's terminology of microcomputer, minicomputer, etc., provides no clear separation among what are commonly thought to be different classes of machines. The only consistent definition appears to be based on physical size. For Instance:

A microcomputer = 100 cm^3
A minicomputer = 1,000 cm^3
A midicomputer = 1 m^3
A computer (IBM) = 10 m^3
A super computer = 100 m^3

This list can be verified by the fact that some minicomputers can out-perform some of the larger conventional full-scale computers. Likewise, microcomputer performance is approaching that of the simplier minicomputers.

The significant characteristics of a computer/memory controller are: A) Size of the memory controlled in words, B) Width of the memory word in bits, C) Memory speed, D) Efficiency of moving and combining data within the memory for the intended range of applications, and E) Any peculiar restrictions on I/O device attachment, such as limitations on the number of I/O devices which may be physically attached, special I/O device instructions for addressing the I/O device registers rather than having them appear as memory locations, etc.

Most current computers/memory controllers have the general structure shown in Figure 1. Computers move and combine data in memory according to a list of instruction words stored in the same memory. Each computer has a program counter which defines the address of the next instructions to be executed, and an instruction register which holds the instruction word for the current instruction being executed. In addition, there is a general purpose register file, typically 2 to 16 registers, for temporary storage of memory data and addresses. The execution control logic of a computer performs the following sequence of operations:

1) The program counter is sent to memory as an address to get the next instruction to be executed.

2) The contents of the memory at that address are loaded into the instruction register.

3) The program counter is incremented to the address of the next instructions on the list.

4) The instruction in the instruction register is executed, which may take many steps and involve many transfers between the memory and general register file.

Upon completion of instruction execution (Step 4), the sequence repeats beginning with Step 1.

We must now define the operations that our computer/memory controller can perform. Figure 2 gives a basic instruction set for a computer of the structure shown in Figure 1. A computer that can execute the instructions listed in Figure 2 will be as powerful as the average minicomputer on the market today. It is possible to have instruction sets which are shorter than this, where several instructions are used to achieve the result of one of the instructions shown in Figure 2. Likewise, there are instruction sets considerbly longer than this, where the additional instructions perform in one step an operation which would require several instructions of they type shown in Figure 2.

The instruction set of Figure 2 includes instructions which: (1) Load a general purpose register from memory, (2) Store a general purpose register to memory, and (3) Combine two general purpose registers in various fashions. There are also instructions which modify the contents of the program counter which define the location of the next instruction to be executed. These include: (1) Direct load of the program counter with a new value, (2) Load of the program counter with a new value while saving the old value, and (3) Conditionally loading the program counter depending upon the status of various machine indicators. Last, there is an interrupt instruction which allows an external device to halt the machine and change the contents of the program counter while saving the old value. Note that no instructions have been included for hardware input and output: Individual registers for hardware input and output are assumed to have memory addresses to that input and output operations appear no different from other transfers between the general purpose registers and memory. This technique is currently in wide use in the Digital Equipment Corporation PDP-11 minicomputer.

To those unfamiliar with computer operations, the interrupt feature on a computer/memory controller often seems mysterious. Its operation and use are, however, quite simple. The function of an interrupt is to stop the normal circular sequence of instruction fetch and execution, save the program counter value, force a new fixed value into the program counter, and begin execution with this new fixed value. This allows an external device to interrupt the execution of what might be a lengthy program and cause the computer/memory controller to execute a new program, and to do so in such a manner that the computer can pick up where it left off in the old program. This means that the interrupt feature must perform as described above, stopping the computer and inserting the new program counter value corresponding to the program designed to be executed by the interrupting external device, and saving the old program counter value in some fixed location, so that after execution of the new program, the program counter may again be loaded with the old program counter value and continue execution of the original program. Typically the interrupt program will also save the contents of any of the general purpose registers that it may use, so that the computer can resume execution of the original program with all information intact.

One of the best ways to illustrate the above principles is to design a computer/memory controller. One of the first questions which must be asked, is what kind of a memory do we propose to control. If we examine activity in the minicomputer field, popular memory sizes range from minimum of 4096 words up to 32,768 words. The most popular width is 16 bits. Sixteen bits allows specification of memory addresses up to 65,000 words. Thus, the general purpose registers can be used to hold either address or data words, which is very convenient for address calculations. (Most of the current microprocessors are 8 bits. Since 12 to 16 bits are required to specify from 4096 to 32,768 words, respectively, these machines require several program steps or special instruction to do address calculation on 16 bit address words.) Speed of the memory is essentially defined by current technology and is in range of 0.1 to 2.0 microseconds.

Figure 3 shows the block diagram of a 16 bit microprocessor of the structure shown in Figure 1. This particular machine is based on the use of the Monolithic Memories 6701 4 bit microcontroller. Instruction execution logic for this machine is microprogram controlled, which means that the execution sequence is controlled by a counter, and a number of Read Only Memories which decode the counter contents to implement a control sequence.

This machine has been designed to be as straight-forward as possible, with no attempt at optimization. Obvious improvements should occur to the reader as we examine the design. Even so, assuming a semiconductor memory, this machine will perform comparably in speed and power with the best minicomputers.

One of the 16 registers in the 6701's register 15 has been assigned as the program counter. The other 15 registers are used as general purpose registers, corresponding to those shown in Figure 1.

Figure 4 shows detail of the microprogram control for this machine. Microprogram control consists of an 8 bit counter driving six 256 x 4 ROMS. The 16 bit instruction register is divided into 3 fields. The first 5 bits of the 16 bit instruction word are used to define 1 of 32 possible instructions to be executed. The last

8 bits of the instruction are divided into two four bit fields defining the A and B register select inputs on the 6701's. The remaining items consist of a multiplexer, which allows selection of either the A or B fields or binary 15 to be selected as input to the B address on the 6701, a 4 bit status register and conditional branch selection multiplexer, a 16 bit memory address register, and a clock oscillator.

Instruction execution in this microprocessor proceeds as follows. The 8 bit ROM counter is started initially at zero. The control ROMS decode the zero count and cause the program counter, register 15, to be set to the memory address register in preparation for fetch of the next instruction to be executed. This is done by causing the 6701 B input select multiplex to be forced to an all lows condition and enabling the memory address register load pulse. Thus, at the next clock pulse, the contents of register 15, the program counter, will be loaded into the memory address register, and the 8 bit ROM counter will be stepped from zero to 1.

In State 1, the contents of the memory at the location defined by the memory address register, will be put on the Data-In bus. The control ROMS decode the count of 1 and enable the instruction register to be loaded. The clock pulse at the end of State 1 will therefore cause the instruction register to be loaded from Data-In bus with the next instruction to be executed and also step the ROM counter to the count of 2.

In State 2, the Start Count ROM decodes the first 5 bits of the instruction register to produce an 8 bit number which identifies the starting count in the control ROM corresponding to the instruction to be executed. The control ROMs also set up the 6701's to increment register 15, the program counter, in this state. This is done by forcing a register address of 15 and performing a B+Φ+Carry In operation. In State 2 the control ROM enables the 8 bit ROM counter to be loaded by the clock pulse at the end of the state. Let us assume for the moment that the instruction to be executed is a register to register add instruction with a start count of 21. At the end of State 2, the 8 bit ROM counter will therefore be loaded with a count of 21.

In State 21 the control ROMs will decode the count of 21 in the ROM counter and set up the 6701 to perform an A+B to B, ADD function. Also, the control ROMs will set up the Status Multiplexer for an unconditional clear function. This means that the status multiplexer will select a 1 condition and enable the clear gate line to the 74163, 8 bit ROM counter. Since the 74163 is a synchronous clear counter, this means that the ROM counter will be cleared to zero by the clock pulse at the end of State 21. This corresponds to the end of execution of this instruction, since clearning the ROM counter to zero will begin the execution of another instruction fetch sequence as described above.

In review:

State 0	Sent the program counter contents to the memory address register.
State 1	Loaded the next instruction to be executed from memory into the instruction register.
State 2	Incremented the contents of the program counter and prepared to execute the instruction.
State 21	Executed the instruction and prepared to clear the ROM counter for fetch of the next instruction.

All instructions are executed in this manner, beginning with States 0, 1, and 2. Each instruction, however, has its own starting count and may be one or several steps in length before returning to State zero to begin fetch of the next instruction.

Figure 5 shows an instruction set for this machine designed to meet the requirements of the general purpose instruction set outlined in Figure 2. Register load from memory and store to memory instructions use the B field of the instruction to define the register to be loaded and stored. The A field defines the register to be used as the source of the memory address in calculated address instructions. A second word of memory

following the instruction word is used to define the memory address for load and store instructions where the address is defined as part of the instruction: the second word is fetched from memory in a manner similar to the initial fetch of the instruction, and the program counter is incremented to point to the word following this address word for the next instruction to be executed. An additional mode of register load has been added: That of direct load of the contents of this second word into a register rather than using the contents of this word as a memory address.

This instruction set implements the functions defined by the basic computer/memory controller instruction set of Figure 2, including some useful additions. Speed of execution of this machine will be limited by the settling time of the ROM counter and control ROMs, and the settling time of the 6701 for its various operations. A 300ns clocking interval is practical for this machine, and will result in a 1.2 ns, register to register add time for the first sequence described above, assuming a 150ns access time memory.

Figure 6 gives the full microprogram for this machine. Note that only 46 out of the 256 possible steps were used to implement the 19 out of a possible 32 instructions. Applying this microprocessor to specific applications will undoubtedly suggest additional instructions in order to do in one instruction operations which would normally require several of the basic instructions. Some examples of instruction set expansion are shown in Figure 7:

1. An indexed register load and store combines the contents of specified register with contents of the word following the instruction to define the memory address for the data transfer.

2. A byte swap instruction, where a register is shifted on itself 8 spaces, can be convenient for handling 8 bit character data, etc.

At this point, it should be clear that instruction set expansion and customization quickly becomes application oriented and, a memory controller, like any other logic controller, eventually becomes oriented toward particular application areas as the design becomes more sophisticated. The basic instruction set in Figure 4 provides a general purpose capability for the machine. The capability for instruction set expansion provides the option to add instructions to significantly improve overall controller performance in specific application areas. The straightforward design of this computer/memory controller can be improved in several ways. The general method of improvement is to reduce the number of states that are required to fetch and execute each instruction, and to add more powerful instructions (which may require additional hardware to support them) to decrease the amount of time required to perform a function in a given application.

By defining a computer as a memory controller, much of the mystery surrounding computer technology can be removed. It is simply a program controlled logic system that happens to have its program stored in the same unit that it is controlling. This also helps to clarify performance comparisons among various computers. The basic parameters are the size and speed of the memory being controlled, plus suitability of the memory controller for a particular memory application. Suitability means identifying how well the basic instruction set is implemented plus the number and power of the added instructions aimed at particular application areas. For instance: Byte manipulation instructions for character processing, hardware multiply and divide and floating point operations for scientific applications which require considerable classical mathematical calculation, etc.

The purpose of this article is to show you that computers, far from being mysterious and esoteric, are just another example of a relatively simple digital system that happens to have a great deal of capability. So, if the microprocessor you are currently considering for inclusion in your product design is not a very efficient memory controller for your application, why not consider designing your own?!

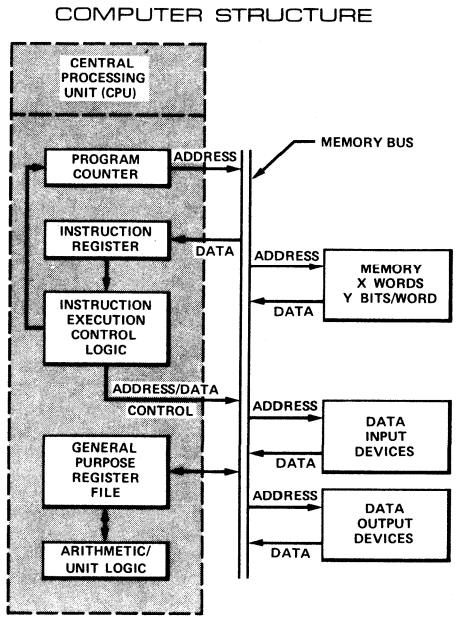

COMPUTER STRUCTURE
CENTRAL PROCESSING UNIT (CPU)
PROGRAM COUNTER
ADDRESS
MEMORY BUS
INSTRUCTION REGISTER
DATA
ADDRESS
MEMORY X WORDS Y BITS/WORD
DATA
INSTRUCTION EXECUTION CONTROL LOGIC
ADDRESS/DATA
CONTROL
ADDRESS
DATA INPUT DEVICES
DATA
GENERAL PURPOSE REGISTER FILE
ADDRESS
DATA OUTPUT DEVICES
DATA
ARITHMETIC/ UNIT LOGIC

FIGURE 1

BASIC COMPUTER INSTRUCTIONS

1. LOAD REGISTER
   a. FROM ADDRESS SPECIFIED BY INSTRUCTION
   b. FROM CALCULATED ADDRESS SPECIFIED BY REGISTER

2. STORE REGISTER
   a. TO SPECIFIED ADDRESS
   b. TO CALCULATED ADDRESS

3. COMBINE REGISTERS
   a. COPY : A → B
   b. ADD : B + A → B
   c. SUBTRACT : B − A → B
   d. AND : B ∧ A → B
   e. OR : B ∨ A → B

4. MODIFY REGISTER : SHIFT
   a. SHIFT LEFT : B × 2 → B
   b. SHIFT RIGHT : B ÷ 2 → B

5. LOAD PROGRAM COUNTER (JUMP)
   a. WITH ADDRESS SPECIFIED BY INSTRUCTION
   b. WITH CALCULATED ADDRESS SPECIFIED BY REGISTER

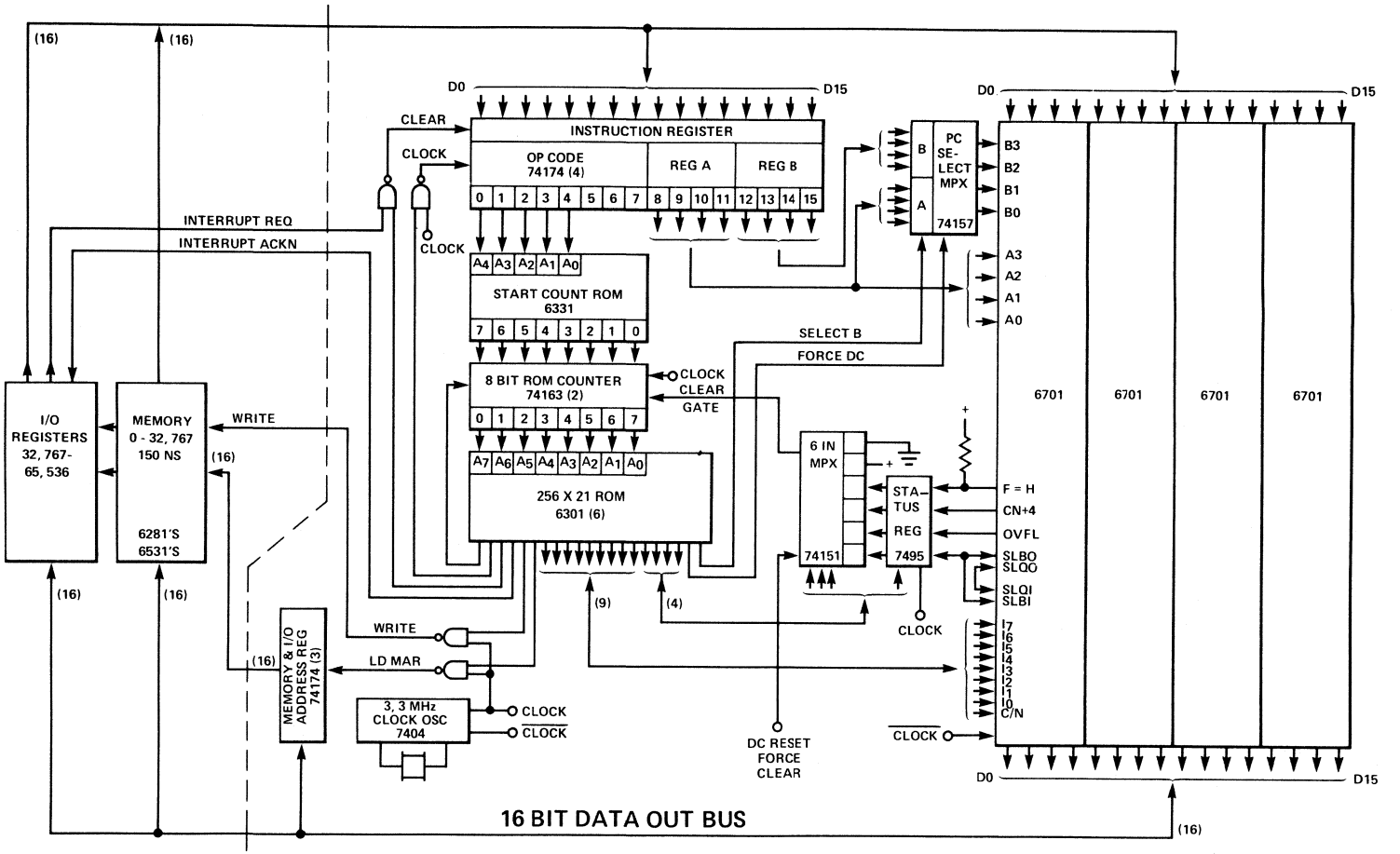
6. LOAD PROGRAM COUNTER AND SAVE OLD VALUE (JUMP TO SUBROUTINE)
   a. WITH ADDRESS SPECIFIED BY INSTRUCTION
   b. WITH CALCULATED ADDRESS SPECIFIED BY REGISTER

7. TEST (RESULT OF PREVIOUS COMBINE OPERATION) AND LOAD P.C. IF :
   a. RESULT WAS ZERO
   b. RESULT WAS NEGATIVE
   c. A CARRY WAS GENERATED

8. INTERRUPT : STORE OLD PC AND LOAD FIXED VALUE

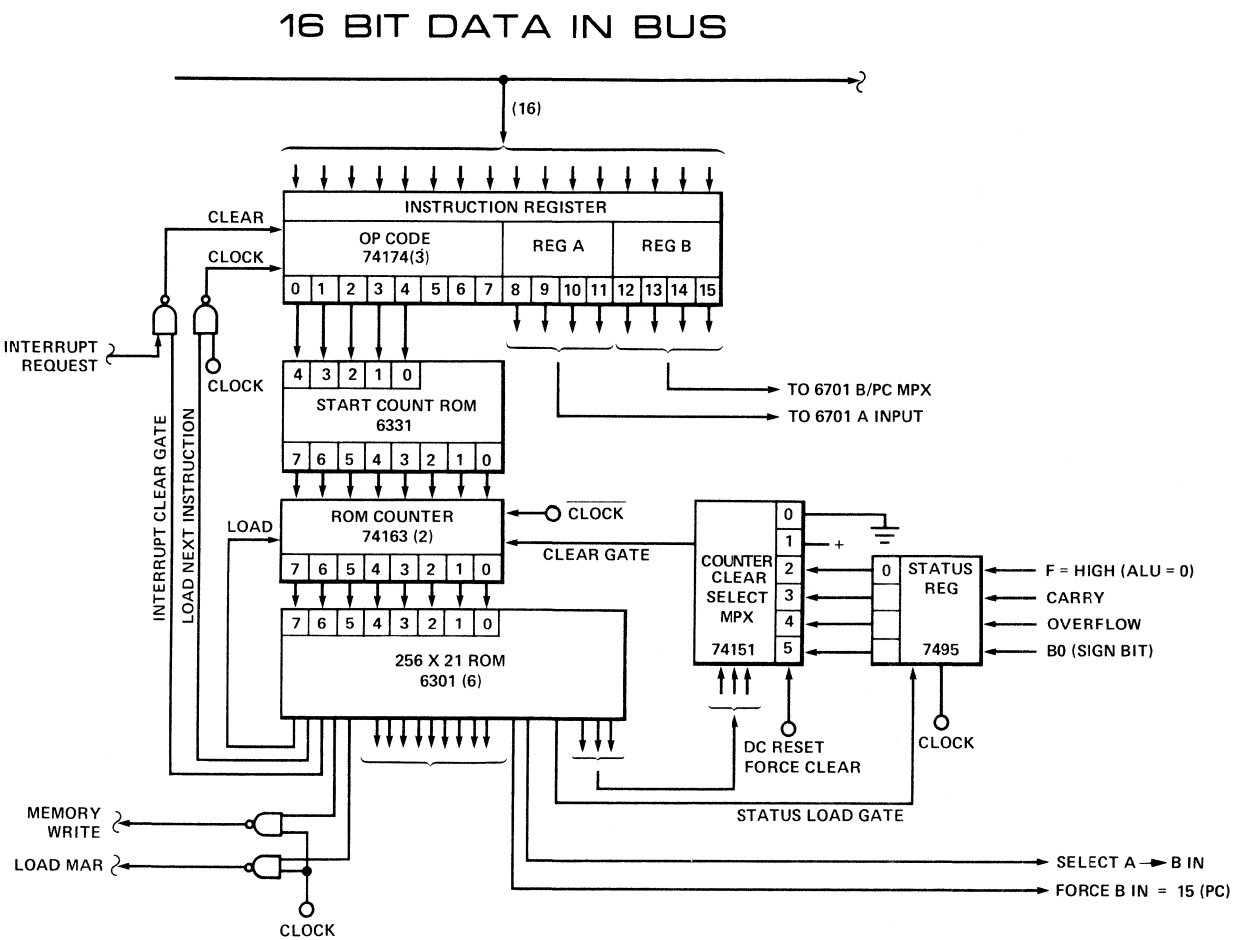
FIGURE 2

6-15



16 BIT MICROPROGRAMMED MICROPROCESSOR
24 CHIPS, 1.20 MICROSEC ADD, 10 WATTS

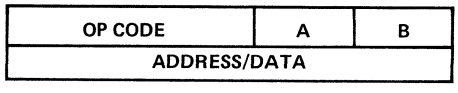
FIGURE 3



16 BIT MICROPROGRAMMED MACHINE CONTROL SECTION

FIGURE 4

SIMPLE 16 BIT MACHINE INSTRUCTION SET



WORD 1
WORD 2
(OPTIONAL)

OP CODE	INSTRUCTION
0	INTERRUPT: STORE PC IN INTERNAL Q REG LOAD PC WITH 0000
1	LOAD REGISTER B, ADDRESS FOLLOWS INSTRUCTION
2	LOAD REGISTER B, ADDRESS IN REGISTER A
3	LOAD REGISTER B, DATA FOLLOWS INSTRUCTION
4	STORE REGISTER B, ADDRESS FOLLOWS INSTRUCTION
5	STORE REGISTER B, ADDRESS IN REGISTER A
6	COPY A TO B : A→B
7	COPY INTERNAL Q REG TO B : Q→B
8	ADD : B + A→B
9	SUBTRACT : B – A→B
10	AND : B A→B
11	OR : B A→B
12	ROTATE LEFT A AND B : A = MOST SIGNIFICANT
13	ROTATE RIGHT A AND B : A = MOST SIGNIFICANT
14	LOAD PC, SAVE OLD PC IN Q, DATA FOLLOWS INSTRUCTION
15	TEST ZERO: LOAD PC IF ZERO FF ON, DATA FOLLOWS
16	TEST SIGN : LOAD PC IF SIGN FF ON, DATA FOLLOWS
17	TEST CARRY : LOAD PC IF CARRY FF ON, DATA FOLLOWS
18	TEST OVERFLOW : LOAD PC IF OVERFLOW FF ON, DATA FOLLOWS
19	UNUSED
1	1
31	UNUSED

FIGURE 5

SIMPLE 16 BIT MACHINE MICROPROGRAM

ROM ADDRESS	OPERATIONS PERFORMED
0	PC → BUS, LOAD MAR
1	PC + 1 → PC, LOAD INSTRUCTION REG
2	LOAD START COUNT → ROM COUNTER
3	OP = 0, INTERRUPT: PC - 1 → Q
4	OP = 0, INTERRUPT: 0000 → PC, END OP
5	OP = 1, LOAD B: PC → MAR
6	OP = 1, LOAD B: PC + 1 → PC
7	OP = 1, LOAD B: MEM + 0 → Q, LOAD MAR
8	OP = 1, LOAD B: MEM → B, END OP
9	OP = 2, LOAD B: A → MAR
10	OP = 2, LOAD B: MEM → B, END OP
11	OP = 3, LOAD B: PC → MAR
12	OP = 3, LOAD B: PC + 1 → PC
13	OP = 3, LOAD B: MEM → B, END OP
14	OP = 4, STORE B: PC → MAR
15	OP = 4, STORE B: PC + 1 → PC
16	OP = 4, STORE B: B → MEM, WRITE, END OP
17	OP = 5, STORE B: A → MAR
18	OP = 5, STORE B: B → MEM, WRITE, END OP
19	OP = 6, COPY A B: A → B, END OP
20	OP = 7, COPY Q B: Q → B, END OP
21	OP = 8, ADD: B + A → B, END OP
22	OP = 9, SUBTRACT: B-A → B, END OP
23	OP = 10, AND: B ∧ A → B, END OP
24	OP = 11, OR: B ∨ A → B, END OP
25	OP = 12, ROTATE LEFT: B → Q
26	OP = 12, ROTATE LEFT: SHIFT LEFT A AND Q
27	OP = 12, ROTATE LEFT: Q → B, END OP
28	OP = 13, ROTATE RIGHT: B → Q
29	OP = 13, ROTATE RIGHT: SHIFT RIGHT A AND Q
30	OP = 13, ROTATE RIGHT: Q → B, END OP
31	OP = 14, LOAD PC & SAVE OLD: PC → MAR
32	OP = 14, LOAD PC & SAVE OLD: PC + 1 → Q
33	OP = 14, LOAD PC & SAVE OLD: MEM → PC, END OP
34	OP = 15, TEST ZERO: PC → MAR
35	OP = 15, TEST ZERO: PC + 1 → PC, END IF ZERO FF OFF
36	OP = 15, TEST ZERO: MEM → PC, END OP
37	OP = 16, TEST SIGN: PC → MAR
38	OP = 16, TEST SIGN: PC + 1 → PC, END IF SIGN FF OFF
39	OP = 16, TEST SIGN: MEM → PC, END OP
40	OP = 17, TEST CARRY: PC → MAR
41	OP = 17, TEST CARRY: PC + 1 → PC, END IF SIGN FF OFF
42	OP = 17, TEST CARRY: MEM → PC, END OP
43	OP = 18, TEST OVERFLOW: PC → MAR
44	OP = 18, TEST OVERFLOW: PC + 1 → PC, END IF OVERFLOW FF OFF
45	OP = 18, TEST OVERFLOW: MEM → PC, END OP
46 ↓	↓ UNUSED
255	UNUSED

FIGURE 6

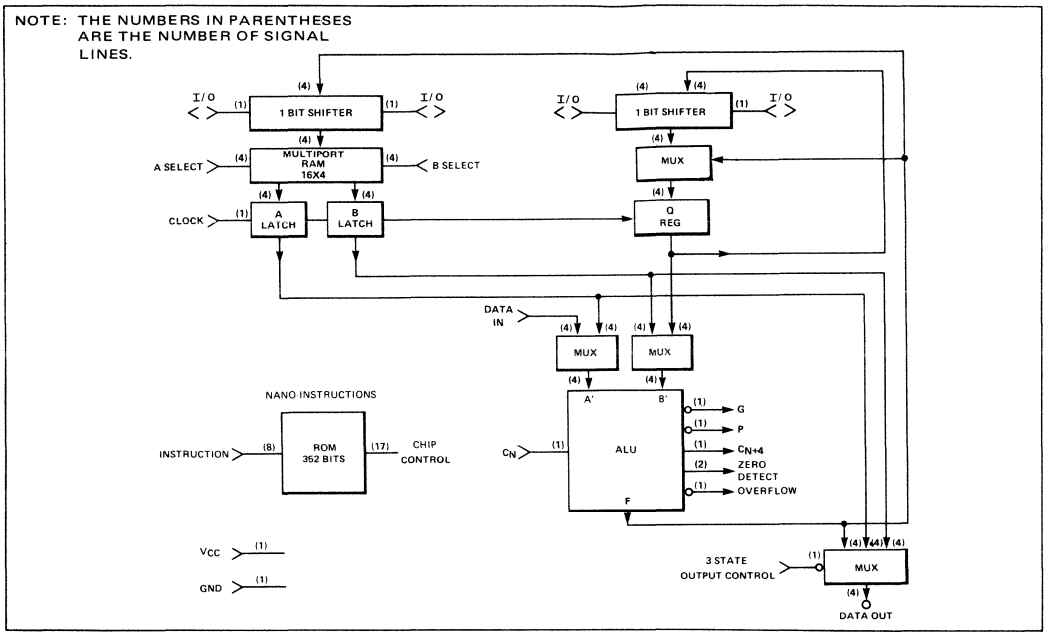
INSTRUCTION SET EXPANSION
TYPICAL EXAMPLES

OP CODE	INSTR
18	LOAD REGISTER B : ADDRESS = (A) + WORD FOLLOWING INSTR
19	STORE REGISTER B : ADDRESS = (A) + WORD FOLLOWING INSTR
20	BYTE SWAP B
21	ARITHMETIC SHIFT RIGHT B : SHIFT IN SIGN
22	INCREMENT B
23	INVERT B
24	ADD CARRY
25	MOVE WORD: FROM ADDRESS IN A TO ADDRESS IN B INCREMENT A & B AFTER
26	PUSH B INTO MEMORY STACK : STACK ADDRESS IN A
27	POP MEMORY STACK INTO B : STACK ADDRESS IN A
28	EXCLUSIVE OR : B $\oplus$ A$\longrightarrow$B
29	ETC. - - -

FIGURE 7

ERRATA bij pag. 157

BLOCK DIAGRAM – 5701/6701



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